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LIGHTNING
365/540/730 AT
PRODUCT
MANUAL

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Quantum Lightning 365/540/730AT
Product Manual

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SERVICE CENTERS

Quantum Service Center
715 Sycamore Avenue
Milpitas, California 95035
Phone: (408) 894-4000
Fax: (408) 894-3218

Quantum Gmbh
Genferstrasse 4B
D-6000 Frankfurt am Main 56
West Germany
Phone: (49) 69-509-1080
Fax: (49) 69-509-10891

Quantum Asia-Pacific Pte. Ltd.
50 Tagore Lane #b1-04
Singapore, 2678
Phone: (65) 450-9333
Fax: (65) 452-2544

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RELEASE DATE	MANUAL PART NUMBER	PAGE NUMBER	REVISIONS
January, 1995	81-106892-02		Second Release
		Page 4-5	Correction made to Table 4-4, Power Reset Limits.
		Page 6-25	Table added showing sector count numbers and time intervals.

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Chapter 1
ABOUT THIS MANUAL

This chapter gives an overview of the contents of this manual, including the intended audience, how the manual is organized, terminology and conventions, and references.

1.1 AUDIENCE DEFINITION

The Quantum Lightning™ 365/545/730AT Product Manual is intended for several audiences. These audiences include: the end user, installer, developer, original equipment manufacturer (OEM), and distributor. The manual provides information about installation, principles of operation, interface command implementation, and maintenance.

1.2 MANUAL ORGANIZATION

This manual is organized into the following chapters:

- Chapter 1 – *About This Manual*
- Chapter 2 – *General Description*
- Chapter 3 – *Installation*
- Chapter 4 – *Specifications*
- Chapter 5 – *Basic Principles of Operation*
- Chapter 6 – *IDE Bus Interface and ATA Commands*

1.3 TERMINOLOGY AND CONVENTIONS

In the Glossary at the back of this manual, you can find definitions for many of the terms used in this manual. In addition, the following abbreviations are used in this manual:

ASIC	application-specific integrated circuit
ATA	Advanced Technology Attachment
bpi	bits per inch
dB	decibels
dBA	decibels, A weighted
ECC	error correcting code
fci	flux changes per inch
Hz	hertz
KB	kilobytes

• LSB	least significant bit
• mA	milliamperes
• MB	megabytes (1 MB = 1,000,000 bytes when referring to disk storage and 1,048,576 bytes in all other cases)
• Mbit/s	megabits per second
• MB/s	megabytes per second
• MHz	megahertz
• ms	milliseconds
• MSB	most significant bit
• mv	millivolts
• ns	nanoseconds
• tpi	tracks per inch
• µs	microseconds
• V	volts

The typographical and naming conventions used in this manual are listed below. Conventions that are unique to a specific table appear in the notes that follow that table.

Typographical Conventions:

- **Names of Bits:** Bit names are presented in initial capitals. An example is the Host Software Reset bit.
- **Commands:** Firmware commands are listed in all capitals. An example is WRITE LONG.
- **Register Names:** Registers are given in this manual with initial capitals. An example is the Alternate Status Register.
- **Parameters:** Parameters are given as initial capitals when spelled out, and are given as all capitals when abbreviated. Examples are Prefetch Enable (PE), and Cache Enable (CE).
- **Hexadecimal Notation:** The hexadecimal notation is a lower-case "h." An example is 30h.
- **Signal Negation:** A signal name that is defined as active low is listed with a minus sign following the signal. An example is RD–.
- **Messages:** A message that is sent from the drive to the host is listed in all capitals. An example is ILLEGAL COMMAND.

Naming Conventions:

- **Host:** In general, the system in which the drive resides is referred to as the host.
- **Computer Voice:** This refers to items you type at the computer keyboard. These items are listed in 10-point, all capitals, Courier font. An example is `FORMAT C:/S.`

1.4 REFERENCES

For additional information about the AT interface, refer to:

- IBM Technical Reference Manual #6183355, March 1986.
- ATA Common Access Method Specification, Revision 4.0.

Chapter 2
GENERAL DESCRIPTION

This chapter summarizes the general functions and key features of the Quantum Lightning™ 365/540/730AT hard disk drives, as well as the applicable standards and regulations.

2.1 PRODUCT OVERVIEW

Quantum's Lightning hard disk drives are part of a family of high performance, 1-inch-high hard disk drives manufactured to meet the highest product quality standards.

These hard disk drives use nonremovable, 3 1/2-inch hard disks and are available with either a Small Computer System Interface (SCSI-2, 3) or ATA interface. A Lightning 365/540/730AT hard disk drive is compatible with systems that provide the IDE interface.

The Lightning 365/540/730AT hard disk drives feature an embedded hard disk drive controller and use ATA commands to optimize system performance. Because the drive manages media defects and error recovery internally, these operations are fully transparent to the user.

The innovative design of the Lightning 365/540/730AT hard disk drives enables Quantum to produce a family of low-cost, high-reliability drives.

2.2 KEY FEATURES

The Lightning 365/540/730AT hard disk drive includes the following key features:

General

- Formatted storage capacity of 365 MB (1 disk, 2 heads), 540 MB (2 disks, 3 heads) or 730 MB (2 disks, 4 heads)
- Low profile, 1-inch height
- Industry standard 3 1/2-inch form factor
- Emulation of IBM® PC AT® task file register, and all AT fixed disk commands

Performance

- Average seek time of 11.5 ms
- Average rotational latency of 6.7 ms
- 128K buffer with 96K dynamic segmentation cache. Look-ahead DisCache feature with continuous prefetch and WriteCache write-buffering capabilities
- AutoRead, AutoWrite, and AutoTransfer features in a custom ASIC
- Read-on-arrival firmware
- ECC on-the-fly

- 1:1 interleave on read/write operations
- Support of all ATA data transfer modes including local bus timing
- Data transfer rate of up to 6.0 MB/s using programmed I/O without IORDY, up to 11 MB/s using programmed I/O with IORDY, and 13 MB/s using multiword DMA

Reliability

- 300,000 hour mean time between failure (MTBF) in the field
- Automatic retry on read errors
- 112-bit, interleaved Reed-Solomon Error Correcting Code (ECC), with double burst correction for bursts up to 48 bits in length
- Self-diagnostic firmware
- Patented Airlock® automatic shipping lock and dedicated landing zone
- Transparent media defect mapping
- High performance, in-line defective sector skipping
- Adaptive cache segmentation
- Reassignment of defective sectors discovered in the field, without reformatting

Versatility

- Power saving modes
- Downloadable firmware
- Cable select feature
- Ability to daisy-chain two drives on the interface

2.3 STANDARDS AND REGULATIONS

The Lightning 365/540/730AT hard disk drive satisfies the following standards and regulations:

- Underwriters Laboratory (U.L.): Standard 1950. Information technology equipment including business equipment.
- Canadian Standards Association (CSA): Standard C22.2 No. 950-M89. Information technology equipment including business equipment.
- European Standards (VDE and TUV): Standard EN 60 950. Information technology equipment including business equipment.
- Federal Communications Commission (FCC): FCC Rules for Radiated and Conducted Emissions, Part 15, Sub Part J, For Class B Equipment.

2.4 HARDWARE REQUIREMENTS

The Lightning 365/540/730AT hard disk drive is compatible with the IBM PC AT and other computers that are compatible with the IBM PC AT. It connects to the PC either by means of a third-party IDE-compatible adapter board, or by plugging a cable from the drive directly into a PC motherboard that supplies an IDE interface.

Chapter 3
INSTALLATION

This chapter explains how to unpack, configure, mount, and connect the Lightning 365/540/730AT hard disk drive prior to operation. It also explains how to start up and operate the drive.

3.1 SPACE REQUIREMENTS

Quantum ships the Lightning 365/540/730AT hard disk drive without a faceplate. Figure 3-1 shows the external dimensions of the drive.

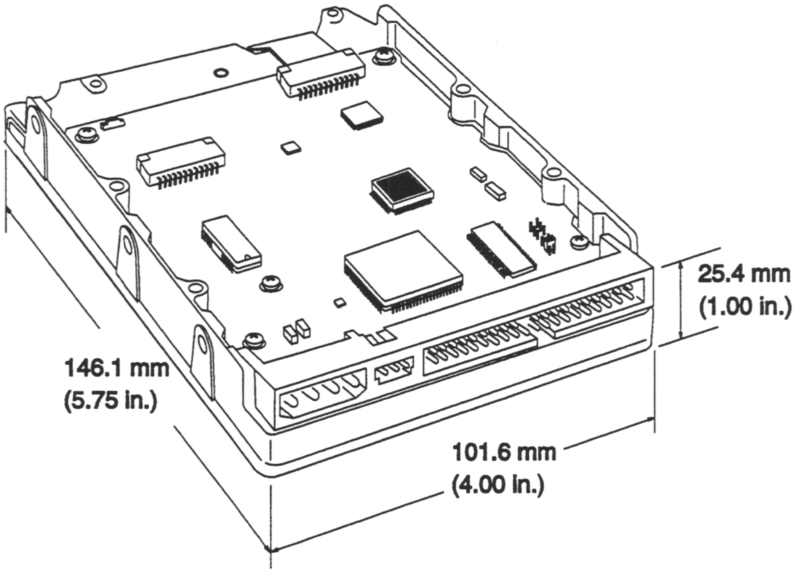

Figure 3-1 *Lightning Mechanical Dimensions*

3.2 UNPACKING INSTRUCTIONS

CAUTION: The maximum limits for physical shock can be exceeded if the drive is not handled properly. Special care should be taken not to bump or drop the drive.

1. Open the shipping container and remove the packing assembly that contains the drive.

2. Remove the drive from the packing assembly.

CAUTION: During shipment and handling, the antistatic electrostatic discharge (ESD) bag prevents electronic component damage due to electrostatic discharge. To avoid accidental damage to the drive, do not use a sharp instrument to open the ESD bag. Save the packing materials for possible future use.

3. When you are ready to install the drive, remove it from the ESD bag.

Figure 3-2 shows the packing assembly for a single Lightning 365/540/730AT hard disk drive. A 12-pack shipping container is available for multiple drive shipments.

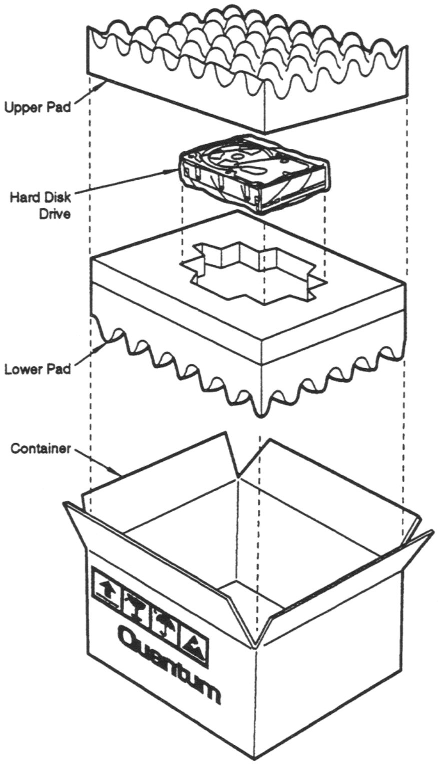

Figure 3-2 *Drive Packing Assembly*

3.3 HARDWARE OPTIONS

The configuration of a Lightning 365/540/730AT hard disk drive depends on the host system in which it is to be installed. This section describes the hardware options that you must take into account prior to installation. Figure 3-3 shows the printed circuit board (PCB) assembly, indicating the jumpers that control some of these options.

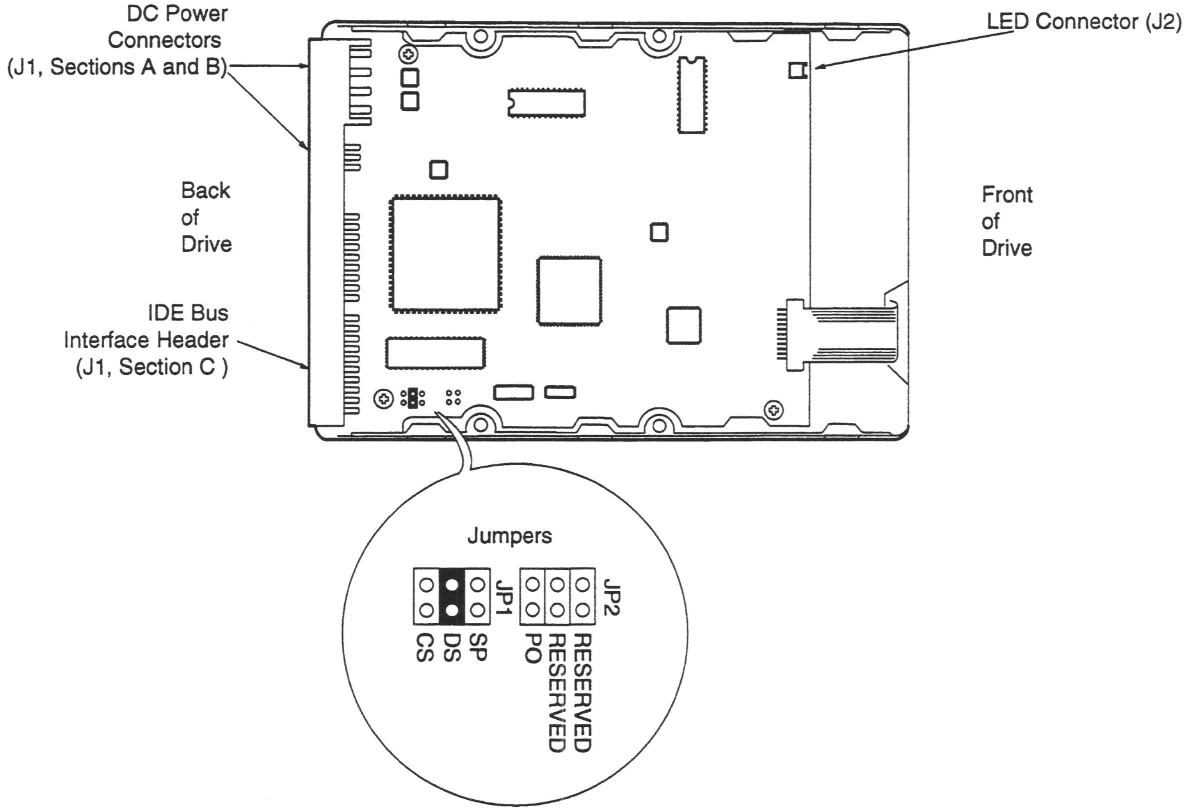
DC Power Connectors (J1, Sections A and B)
LED Connector (J2)
Back of Drive
Front of Drive
IDE Bus Interface Header (J1, Section C)
Jumpers
JP1
JP2
CS
DS
SP
PO
RESERVED
RESERVED

Figure 3-3 *Jumper Locations on the Drive PCB*

The configuration of the following four jumpers controls the drive's mode of operation:

- CS – Cable Select
- DS – Drive Select
- SP – Slave Present
- PO – Product Option

Table 3-1 defines the jumper configurations for the drive and the operational modes that result from the configurations. *1* indicates that the specified jumper is installed; *0* indicates that the jumper is not installed.

Table 3-1 *Jumper Options*

CS	DS	SP	DESCRIPTION
0	0	0	Slave Drive. Compatible with drives using the PDIAG– line to handle Master/Slave communications.
0*	1*	0*	Master drive (or single drive). Uses DASP– to check for the presence of a Slave.
0	1	1	Master Drive (in PDIAG– mode). Uses the SP jumper to determine whether a Slave is present, without checking DASP–.
1	0	X	Slave or Master Drive, depending on the state of the Quantum Cable Select signal (pin 28) at the AT-bus connector. If the Cable Select signal is set to 0 (grounded), then the drive is configured as if DS were 1, described earlier. If the Cable Select signal is set to 1 (high), then the drive is configured as if DS were 0, described earlier.

Note: In Table 3-1, a *0* indicates that the jumper is removed; a *1* indicates that the jumper is installed. The asterisk (*) indicates factory default settings.

CAUTION: The CS and DS jumpers should not be installed at the same time.

3.3.1 Cable Select (CS) Jumper

When two Lightning 365/540/730AT hard disk drives are daisy-chained together, they can be configured as Master or Slave either by the CS or DS jumpers. Only one jumper may be used at a time. To configure the drive as a Master or Slave with the CS feature, the CS jumper is installed (1) and the DS jumper is removed (0).

Once you install the CS jumper, the drive is configured as a Master or Slave by the state of the Cable Select signal: pin 28 of the IDE bus connector. Please note that pin 28 is a vendor-specific pin that Quantum is using for a specific purpose. More than one function is allocated to CS, according to the ATA CAM specification (see reference to this specification in Chapter 1). If pin 28 is a *0* (grounded), the drive is configured as a Master. If it is a *1* (high), the drive is configured as a Slave. In order to configure two drives in a Master/Slave relationship using the CS jumper, you need to use a cable that provides the proper signal level at pin 28 of the IDE bus connector. Figure 3-4 provides information on how the CS and DS jumpers are connected.

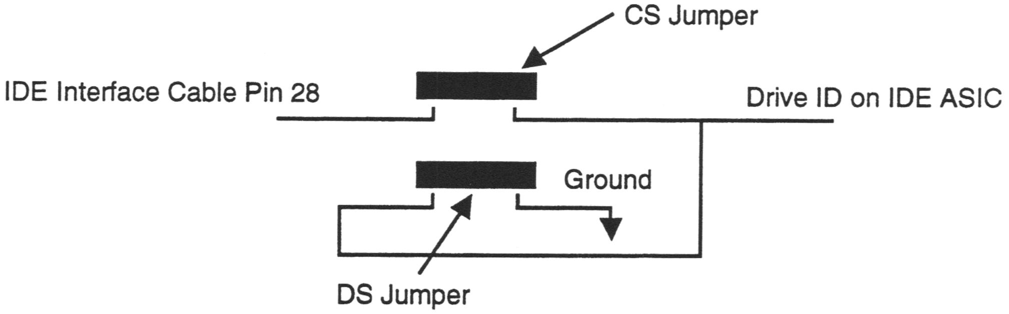

Figure 3-4 *Cable Select Feature*

This allows two drives to operate in a Master/Slave relationship according to the drive cable placement.

3.3.2 Drive Select (DS) Jumper

You can also daisy-chain two drives on the IDE bus interface by using their Drive Select (DS) jumpers. If the DS jumper is installed, the CS jumper must be removed.

To configure a drive as the Master (Drive 0), a jumper must be installed on the DS pins.

Quantum ships the Lightning 365/540/730AT hard disk drives from the factory as a Master (Drive 0 - DS jumper installed). To configure a drive as a Slave (Drive 1), the DS jumper must be removed.

Note: The order in which drives are connected in a daisy chain has no significance.

3.3.3 Slave Present (SP) Jumper

In combination with the current DS or CS jumper settings, the Slave Present (SP) jumper implements one of two possible configurations:

- When the drive is configured as a Master (DS jumper installed **or** CS jumper installed and the Cable Select signal set to *0*) the SP jumper indicates to the drive that a Slave drive is present. The SP jumper should be installed on the Master drive only if the Slave drive does *not* use the Drive Active/Slave Present (DASP–) signal to indicate its presence.
- When the drive is configured as a Slave (DS jumper not installed) the SP jumper enables the self-seek test. When power is applied to the drive with the self-seek test enabled, the drive executes seeks in a *butterfly* pattern.
- If an error is encountered during the self-seek test, the test terminates.

3.3.4 Product Option (PO) Jumper

The PO jumper is reserved for use by specific customers. Do not install the PO jumper for normal IDE Master/Slave operation.

3.4 IDE BUS ADAPTER

There are two ways you can configure a system to allow the Lightning 365/540/730AT hard disk drive to communicate over the IDE bus of an IBM or IBM-compatible PC:

1. Connect the drive to a 40-pin IDE bus connector (if available) on the motherboard of the PC.
2. Install an IDE-compatible adapter board in the PC and connect the drive to the adapter board.

3.4.1 40-Pin IDE Bus Connector

Many of the later design PC motherboards have a built-in 40-pin IDE bus connector that is compatible with the 40-pin IDE interface of the Lightning 365/540/730AT hard disk drive. If the motherboard has an IDE connector, simply connect a 40-pin ribbon cable between the drive and the motherboard.

You should also refer to the motherboard instruction manual and refer to Chapter 6 of this manual to ensure signal compatibility.

3.4.2 Adapter Board

If your PC motherboard does not contain a built-in, 40-pin IDE bus interface connector, you must install an IDE bus adapter board and connecting cable to allow the drive to interface with the motherboard. Quantum does not supply such an adapter board, but they are available from several third-party vendors.

Please carefully read the instruction manual that comes with your adapter board as well as Chapter 6 of this manual to ensure signal compatibility between the adapter board and the drive. Also, make sure that the adapter board jumper settings are appropriate.

3.5 MOUNTING

Drive mounting orientation, clearance, and ventilation requirements are described in the following subsections.

3.5.1 Orientation

The mounting holes on the Lightning 365/540/730AT hard disk drive allow the drive to be mounted in any orientation. Figure 3-5 shows the location of the three mounting holes on each side of the drive. The drive also can be mounted using the four mounting hole locations on the PCB side of the drive.

All dimensions are in millimeters. For mounting, #6-32 UNC screws are recommended.

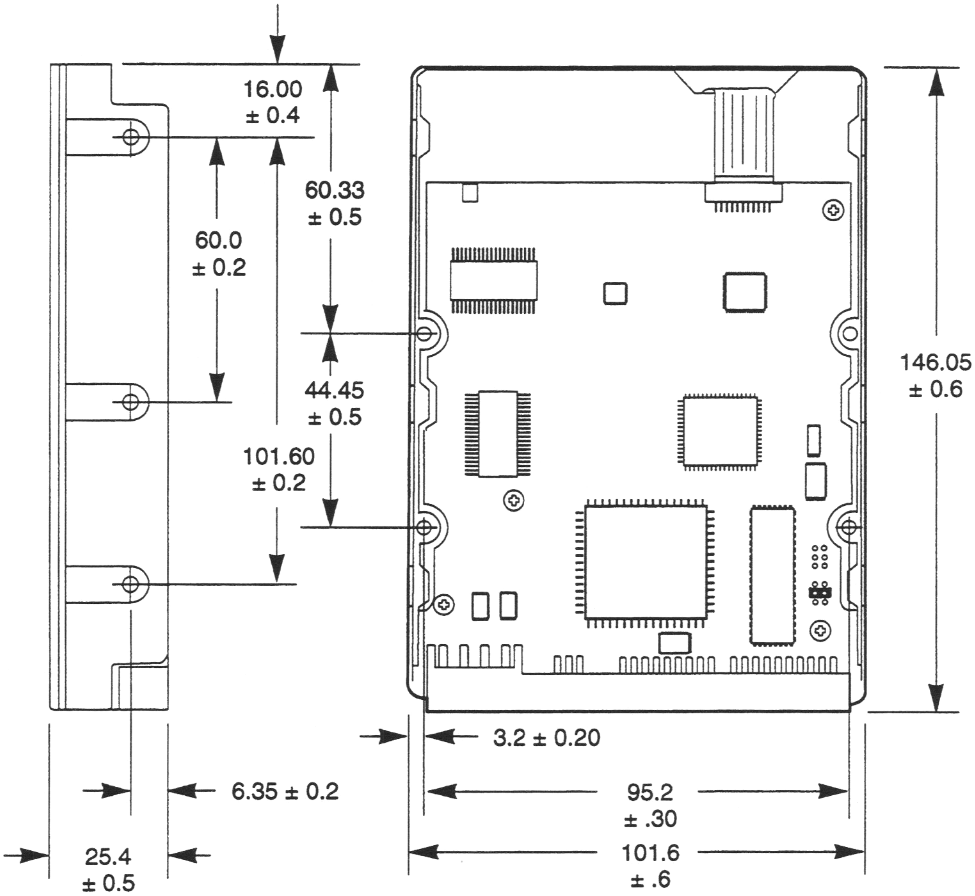

Figure 3-5 *Lightning Mounting Dimensions (in Millimeters)*

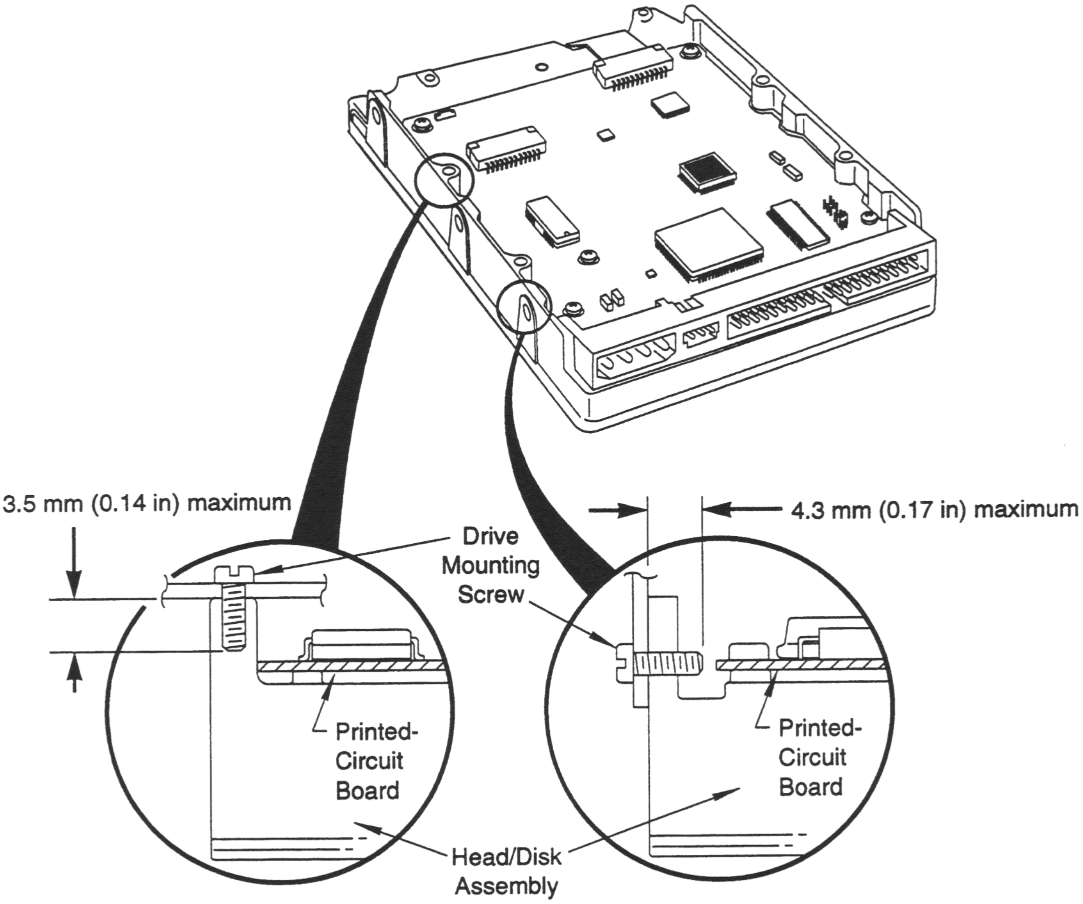

Figure 3-6 *Mounting Screw Clearance*

CAUTION:	The PCB is very close to the mounting holes. Do not exceed the specified length for the mounting screws. The specified screw length allows full use of the mounting hole threads, while avoiding damaging or placing unwanted stress on the PCB. Figure 3-6 specifies the minimum clearance between the PCB and the screws in the mounting holes. To avoid stripping the mounting hole threads, the maximum torque applied to the screws must not exceed 8 inch-pounds.

3.5.2 Clearance

Clearance from the drive to any other surface (except mounting surfaces) must be a minimum of 0.05 inches.

3.5.3 Ventilation

The Lightning 365/540/730AT hard disk drive operates without a cooling fan, provided the ambient air temperature does not exceed 131°F (55°C).

3.6 COMBINATION CONNECTOR (J1)

J1 is a three section combination connector. The drive's DC power can be applied to either section A or B. The IDE bus interface (40-pin) uses section C. The connector is mounted on the back edge of the printed-circuit board (PCB), as shown in Figure 3-7.

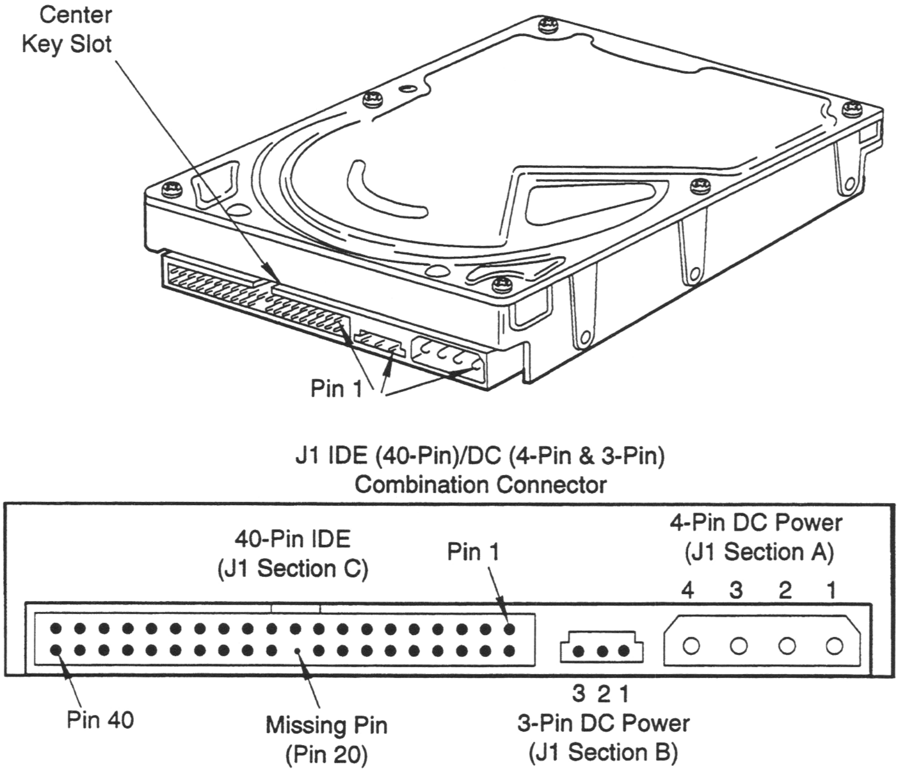
Center Key Slot
Pin 1
J1 IDE (40-Pin)/DC (4-Pin & 3-Pin) Combination Connector
40-Pin IDE (J1 Section C)
Pin 1
4-Pin DC Power (J1 Section A)
4 3 2 1
3 2 1
Pin 40
Missing Pin (Pin 20)
3-Pin DC Power (J1 Section B)

Figure 3-7 *J1 DC Power and IDE Bus Combination Connector*

3.6.1 DC Power (J1, Sections A and B)

The recommended mating connectors for the +5 Vdc and +12 Vdc input power are listed in Table 3-2.

Table 3-2 *J1 Power Connector, Sections A and B*

PIN NUMBER	VOLTAGE LEVEL	MATING CONNECTOR TYPE AND PART NUMBER (OR EQUIVALENT)
J1 Section A (4-Pin):		
1	+12 VDC	4-Pin Connector: AMP P/N 1-480424-0 Loose piece contacts: AMP P/N VS 60619-4 Strip contacts: AMP P/N VS 61117-4
2	Ground Return for +12 VDC	
3	Ground Return for +5 VDC	
4	+5 VDC	
J1 Section B (3-Pin):		
1	+5 Vdc	3-Pin Connector: Molex P/N 5484 39-27-0032
2	+12 Vdc	
3	Ground	

Note: Power can be applied to either J1, sections A or B. Labels indicate the pin numbers on the connector. Pins 2 and 3 of section A are the +5 and +12 volt returns and are connected together on the drive.

3.6.2 LED Connector (J2)

The LED connector may be used to connect an external LED for the purpose of monitoring drive activity. A 220-ohm resistor is connected in series from the +LED pin to +5 volts. The -LED pin is connected to a switching transistor on the drive that turns on and lights the LED when the disk is performing a read or write operation. When no read or write operation is taking place, the transistor turns off and the LED is extinguished. The recommended mating connector parts are shown in Table 3-3.

Table 3-3 *J2 LED Connector*

J2 PINS		MATING CONNECTOR TYPE AND PART NUMBER (OR EQUIVALENT)
PIN NUMBER	FUNCTION	
1	–LED	Two-position housing: Molex P/N 51021-0200 Loose-piece contacts: Molex P/N 50058-8100
2	+LED	

3.6.3 IDE Bus Interface Connector (J1, Section C)

On the Lightning 365/540/730AT hard disk drive, the IDE bus interface cable connector (J1, section C) is a 40-pin Universal Header, as shown in Figure 3-7.

To prevent the possibility of incorrect installation, the connector has been keyed by removing Pin 20. This ensures that a connector cannot be installed upside down.

See Chapter 6, "IDE Bus Interface and ATA Commands," for more detailed information about the required signals. Refer to for the pin assignments of the IDE bus connector (J1, section C).

3.7 FOR SYSTEMS WITH A MOTHERBOARD IDE ADAPTER

You can install the Lightning 365/540/730AT hard disk drive in an AT-compatible system that contains a 40-pin IDE bus connector on the motherboard.

To connect the drive to the motherboard, use a 40-pin ribbon cable 18 inches in length or shorter. Ensure that pin 1 of the drive is connected to pin 1 of the motherboard connector.

3.8 FOR SYSTEMS WITH AN IDE ADAPTER BOARD

To install a Lightning 365/540/730AT hard disk drive in an AT-compatible system without a 40-pin IDE bus connector on its motherboard, you need a third-party IDE-compatible adapter board.

3.8.1 Adapter Board Installation

Carefully read the manual that accompanies your adapter board before installing it. Make sure that all the jumpers are set properly and that there are no address or signal conflicts. You must also investigate to see if your AT-compatible system contains a combination floppy and hard disk controller board. If it does, you must disable the hard disk drive controller functions on that controller board before proceeding.

Once you have disabled the hard disk drive controller functions on the floppy/hard drive controller, install the adapter board. Again, make sure that you have set all jumper straps on the adapter board to avoid addressing and signal conflicts.

3.8.1.1 Connecting the Adapter Board and the Drive

Use a 40-pin ribbon cable to connect the drive to the board. See Figure 3-8. To connect the drive to the board:

1. Insert the 40-pin cable connector into the mating connector of the adapter board. Make sure that pin 1 of the connector matches with pin 1 on the cable.
2. Insert the other end of the cable into the header on the drive. When inserting this end of the cable, make sure that pin 1 of the cable connects to pin 1 of the drive connector.
3. Secure the drive to the system chassis by using the mounting screws, as shown in Figure 3-9.

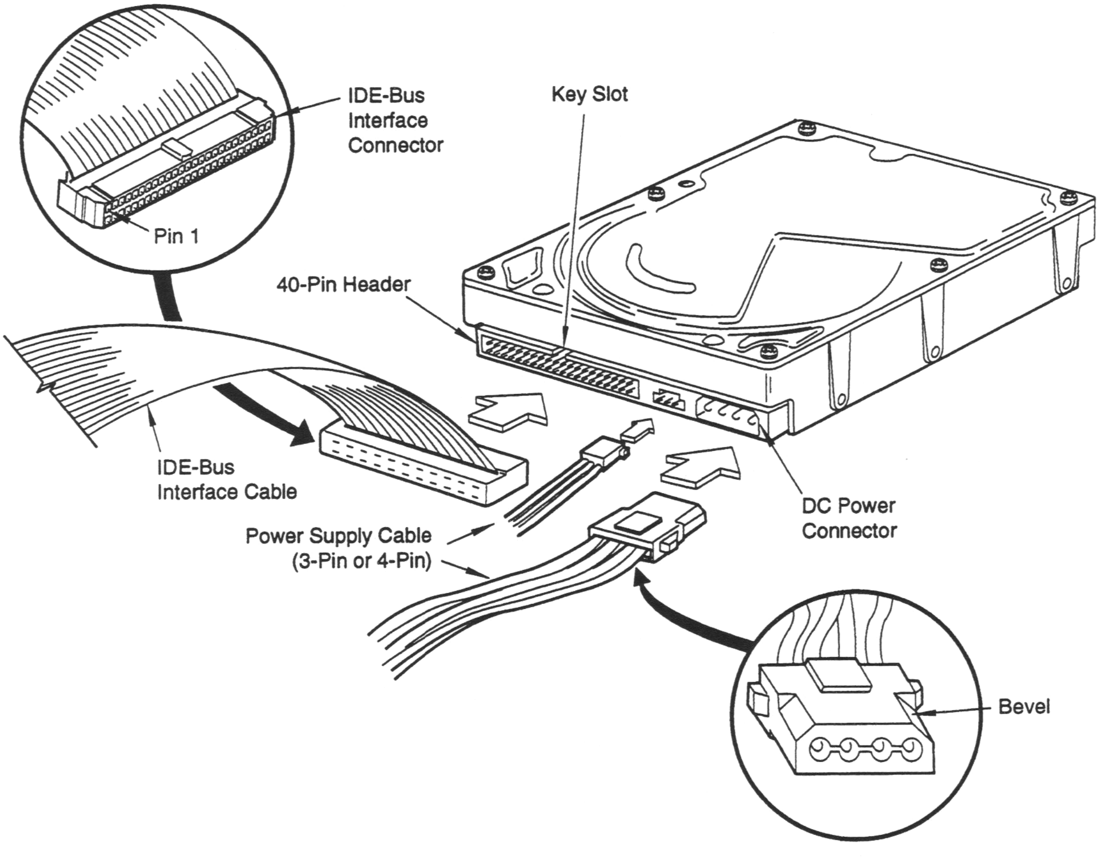

Figure 3-8 *Drive Power Supply and IDE Bus Interface Cables*

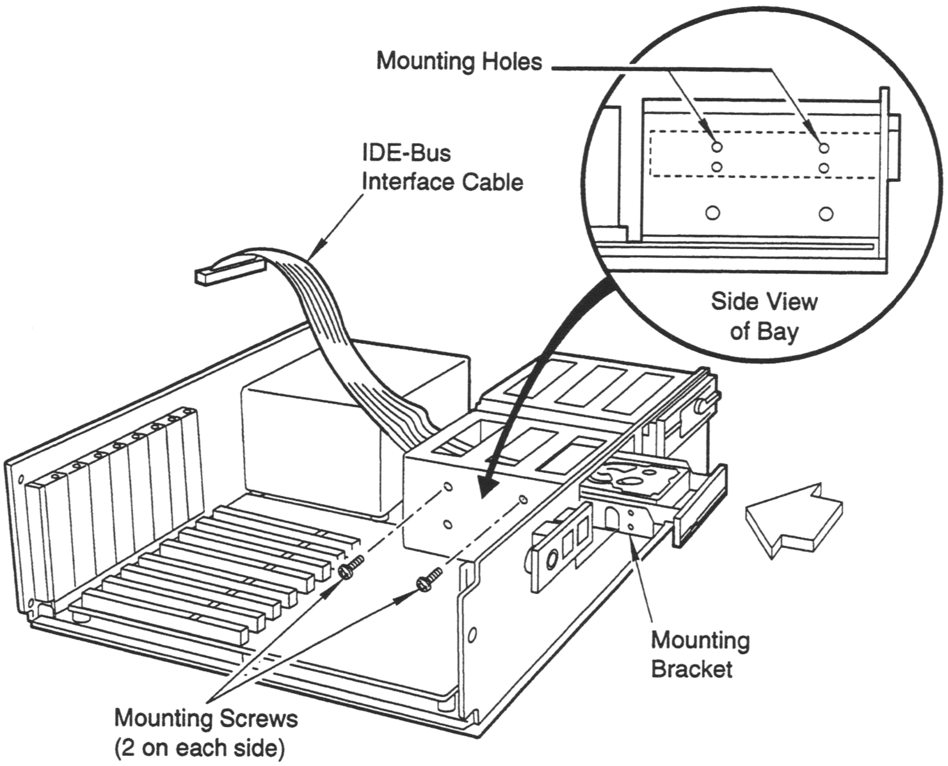

Figure 3-9 *Completing the Drive Installation*

3.9 SYSTEM STARTUP AND OPERATION

Once you have installed the Lightning 365/540/730AT hard disk drive and adapter board (if required) in the host system, you are ready to partition and format the drive for operation. To set up the drive correctly, follow these steps:

1. Power on the system.
2. Run the SETUP program. This is generally on a Diagnostics or Utilities disk, or within the system's BIOS.
3. Enter the appropriate parameters.

   The SETUP program allows you to enter the types of optional hardware installed—such as the hard disk drive type, the floppy disk drive capacity, and the display adapter type. The system's BIOS uses this information to initialize the system when the power is switched on. For instructions on how to use the SETUP program, refer to the system manual for your PC.

   During the AT system CMOS setup, you must enter the drive type for the Lightning 365/540/730AT hard disk drive. The drive supports the translation of its *physical* drive geometry parameters such as cylinders, heads, and sectors per track, to a *logical* addressing mode. The drive can work with different BIOS drive-type tables of the various host systems.

   You can choose any drive type that does not exceed the capacity of the drive. Table 3-4 gives the logical parameters that provide the maximum capacity on the Lightning 365/540/730AT hard disk drives.

Table 3-4 *Logical Addressing Format*

	LIGHTNING 365AT	**LIGHTNING 540AT**	**LIGHTNING 730AT**
Logical Cylinders	976	1,120	1,416
Logical Heads	12	16	16
Logical Sectors/Track	61	59	63
Total Number Logical Sectors	714,432	1,057,280	1,427,328

To match the logical specifications of the drive to the drive type of a particular BIOS, consult the system's drive-type table. This table specifies the number of cylinders, heads, and sectors for a particular drive type.

Note: The BIOS of some systems may not support a logical cylinder value greater than 1,024, as is needed for taking advantage of the maximum capacity of a Lightning 540 or 730AT hard disk drive. For such systems, use a device driver or run in LBA mode if the system BIOS supports it.

You must choose a drive type that meets the following requirements:

For the 365AT:

Logical Cylinders x Logical Heads x Logical Sectors/Track x 512 <= 365,789,184

For the 540AT:

Logical Cylinders x Logical Heads x Logical Sectors/Track x 512 <= 541,327,360

For the 730AT:

Logical Cylinders x Logical Heads x Logical Sectors/Track x 512 <= 730,791,936

4. Boot the system using the operating system installation disk—for example, *MS-DOS*—then follow the installation instructions in the operating system manual.

If you are using a version of MS-DOS below 4.01:

1. Run FDISK or a third-party partitioning program.

Note: If you use DOS version 3.2 or an earlier version, the DOS partition will employ only 32 MB (33,554,432 bytes) of the drive's capacity. With DOS 3.3, you can partition the drive in multiples of 32 MB. If you use DOS 4.01 or later, or if you use a third-party partitioning program, you can create partitions that exceed 32 MB.

2. To format the drive with a high-level format and transfer the operating system to the drive, type `FORMAT C: /S`. Once this command executes, you can boot the system from the hard drive.

Note: The drive is shipped from the factory with a low-level format; therefore, a low-level format is not required.

Chapter 4
SPECIFICATIONS

This chapter gives a detailed description of the physical, electrical, and environmental characteristics of the Lightning 365/540/730AT hard disk drives.

4.1 SPECIFICATION SUMMARY

Table 4-1 gives a summary of the Lightning 365/540/730AT hard disk drive.

Table 4-1 *Specifications*

DESCRIPTION	**LIGHTNING 365AT**	**LIGHTNING 540AT**	**LIGHTNING 730AT**
Capacity (formatted)	365.7 MB	541.3 MB	730.8 MB
Nominal rotational speed (rpm)	4,500	4,500	4,500
Number of disks	1	2	2
Number of R/W heads	2	3	4
Data Organization:			
Zones per surface	15	15	15
Tracks per surface	3,658	3,658	3,658
Total tracks	7,316	10,974	14,632
Sectors per track:			
Inside zone	61	61	61
Outside zone	128	128	128
Total User Sectors	714,432	1,057,280	1,427,328
Bytes per sector	512	512	512
Number of tracks per cylinder	2	3	4
Recording:			
Recording technology	Multiple zone	Multiple Zone	Multiple Zone
Maximum linear density	47,636 fci	47,636 fci	47,636 fci
Encoding method	RLL 1,7	RLL 1,7	RLL 1,7
Interleave	1:1	1:1	1:1
Track density	3,794 tpi	3,794 tpi	3,794 tpi
Maximum effective areal density	241 Mbits/in^2	241 Mbits/in^2	241 Mbits/in^2

DESCRIPTION	LIGHTNING 365AT	LIGHTNING 540AT	LIGHTNING 730AT
Performance:			
Seek times:			
Read-on-arrival	11 ms typ. 12 ms max.	11.5 ms typ. 12.5 ms max.	11.5 ms typ. 12.5 ms max.
Track-to-track	4 ms typical	4 ms typical	4 ms typical
Average write	13 ms	13.5 ms	13.5 ms
Full stroke	19.5 ms typ. 21 ms max.	20.5 ms typ. 21 ms max.	20.5 ms typ. 21 ms max.
Data Transfer rates:			
Disk to Read Buffer[1]	5.9 MB/sec. max.	5.9 MB/sec. max.	5.9 MB/sec. max.
Read Buffer to IDE Bus (PIO Mode w/o IORDY)	6.0 MB/sec. max.	6.0 MB/sec. max.	6.0 MB/sec. max.
Read Buffer to IDE bus (PIO Mode with IORDY)	11.1 MB/sec. max.	11.1 MB/sec. max.	11.1 MB/sec. max.
Read Buffer to IDE bus (DMA Mode)	13.3 MB/sec. max.	13.3 MB/sec. max.	13.3 MB/sec. max.
Buffer size	128 KB	128 KB	128 KB
Reliability:			
Seek error rate[2]	< 1 in 10^6	< 1 in 10^6	< 1 in 10^6
Unrecoverable error rate[2]	< 1 in 10^{14}	< 1 in 10^{14}	< 1 in 10^{14}
Error correction method (with cross check)	112-bit Reed-Solomon	112-bit Reed-Solomon	112-bit Reed-Solomon
Projected MTBF	300,000 hrs	300,000 hrs	300,000 hrs
Contact Start/Stop Cycles	20,000 min.	20,000 min.	20,000 min.
Auto head-park method	AirLock®	AirLock®	AirLock®
Physical characteristics:			
Height	1.00 in (25.4 mm)	1.00 in (25.4 mm)	1.00 in (25.4 mm)
Width	4.0 in (101.6 mm)	4.0 in (101.6 mm)	4.0 in (101.6 mm)
Depth	5.75 in (146.1 mm)	5.75 in (146.1 mm)	5.75 in (146.1 mm)
Weight	1.2 lbs (0.55 kg)	1.2 lbs (0.55 kg)	1.2 lbs (0.55 kg)

1. Disk to read buffer transfer rate is zone dependent.
2. Refer to Section 4.11, "DISK ERRORS" for details on error rate definitions.

4.2 FORMATTED CAPACITY

At the factory, the Lightning 365/540/730AT receives a low-level format that creates the actual tracks and sectors on the drive. Table 4-2 shows the capacity resulting from this process. Formatting done at the user level, for operation with DOS, UNIX, or other operating systems, will result in less capacity than the physical capacity shown in Table 4-2.

Table 4-2 *Formatted Capacity*

	LIGHTNING 365AT	LIGHTNING 540AT	LIGHTNING 730AT
Formatted capacity	365.7 MB[1]	541.3 MB	730.8 MB
Number of 512-byte sectors available	714,432	1,057,280	1,427,328

[1] As defined by Quantum, 1 megabyte (MB) is 10^6, or 1,000,000 bytes.

4.3 DATA TRANSFER RATES

Data is transferred from the disk to the read buffer at a rate up to 5.9 MB/s (47.2 Mbits/s) in bursts. Data is transferred from the read buffer to the IDE bus at a rate of up to 6.0 MB/s using programmed I/O without IORDY, up to 11.1 MB/s using programmed I/O with IORDY, or at a rate of up to 13.3 MB/s using multi-word DMA. For more detailed information on interface timing, refer to Chapter 6.

4.4 TIMING SPECIFICATIONS

Table 4-3 illustrates the timing specifications of the Lightning 365/540/730AT hard disk drive.

Table 4-3 *Timing Specifications*

PARAMETER	TYPICAL NOMINAL[1]	WORST CASE[2]
Sequential Cylinder Switch Time[3]	3.5 ms	5 ms
Sequential Head Switch Time[4]	2 ms	4 ms
Random Average (Read or Seek)	11.5 ms	12.5 ms
Random Average (Write)	13 ms	14 ms
Full-Stroke Seek	19 ms	21 ms
Average Rotational Latency	6.67 ms	—
Power On[5] to Drive Ready[6]	—	12 seconds
Power On to Interface Ready[7]	—	8 seconds
Standby[8] to Interface Ready	—	8 seconds
Drive Ready to Shutdown	5 seconds	20 seconds[9]

1. Nominal conditions are as follows:
    - Nominal temperature 77°F (25° C)
    - Nominal supply voltages (12.0V, 5.0V)
    - No applied shock or vibration
2. Worst case conditions are as follows:
    - Worst case temperature extremes 32 to 131°F (0°C to 55°C)
    - Worst case supply voltages (12V ±10%, 5V±5%)
3. Sequential Cylinder Switch Time is the time from the conclusion of the last sector of a cylinder to the first logical sector on the next cylinder.
4. Sequential Head Switch Time is the time from the last sector of a track to the beginning of the first logical sector of the next track of the same cylinder.
5. Power On is the time from when the supply voltages reach operating range to when the drive is ready to accept any command.
6. Drive Ready is the condition in which the disks are rotating at the rated speed and the drive is able to accept and execute commands requiring disk access without further delay.
7. Interface Ready is the condition in which the drive is ready to accept any command, before the disks are rotating at the rated speed.
8. Standby is the condition in which the microprocessor is powered, but not the HDA. When the host sends the drive a shutdown command, the drive parks the heads away from the data zone and spins down to a complete stop.
9. After 20 seconds, it is safe to move the disk drive.

4.5 POWER

The Lightning 365/540/730AT hard disk drive operates from two supply voltages:

- +12V±10%
- +5V ±5%

The allowable ripple and noise is 100 mV peak-to-peak for the +12 Volt supply and 50 mV peak-to-peak for the +5 Volt supply.

4.5.1 Power Sequencing

You may apply the power in any order or manner, or short or open either the power or power return line with no loss of data or damage to the disk drive. However, data may be lost in the sector being written at the time of power loss. The drive can withstand transient voltages of +10% to –100% from nominal while powering up or down.

4.5.2 Power Reset Limits

When powering up, the drive remains reset (inactive) until both V_{HT} reset limits inTable 4-4 are exceeded. When powering down, the drive becomes reset when either supply voltage drops below the V_{LT} threshold.

Table 4-4 *Power Reset Limits*

DC SUPPLY	5 V	12 V
V_{LT}	4.65 V (max.)[1] 4.29 V (min.)	10.60 V (max.)[1] 9.37 V (min.)
V_{HT}	4.75 V (max.) 4.29 V (min.)	10.83 V (max.) 9.36 V (min.)
Hysteresis	50 mV (min.)	14 mV (min.)

[1] Includes a 100mV peak-to-peak ripple on +5 V or 250 mV peak-to-peak ripple on +12 V to maximize or minimize values.

4.5.3 Power Requirements

Table 4-5 lists the voltages and typical average corresponding currents for the various modes of operation of the Lightning 365/540/730AT hard disk drive.

Table 4-5 *Typical Power and Current Consumption*

MODE OF OPERATION	TYPICAL AVERAGE CURRENT[1] (MA RMS UNLESS OTHERWISE NOTED)						TYPICAL AVERAGE POWER[2] (WATTS)		
	+12 V			+5 V					
MODEL NUMBER	**365**	**540**	**730**	**365**	**540**	**730**	**365**	**540**	**730**
Startup[1] (peak)	919	914	914	452	445	445	13.29	13.19	13.19
Idle[3]	189	215	215	200	195	195	3.27	3.56	3.56
Read/Write/Seek[4]	317	338	338	431	428	428	5.96	6.20	6.20
Maximum Seeking[5]	514	525	525	408	403	403	8.21	8.32	8.32
Standby[6]	15.8	15	15	128	129	129	0.83	0.83	0.83
Sleep[7]	15.8	15	15	128	129	129	0.83	0.83	0.83
Read/Write On Track[8]	186	214	214	446	445	445	4.46	4.79	4.79

1. Startup current is the peak current of peaks greater than 10 ms in duration.
2. Power requirements reflect nominal values for +12v and +5v power
3. Idle mode is in effect when the drive is not reading, writing, seeking, or executing any commands. A portion of the R/W circuitry is powered down, the motor is up to speed and the Drive Ready condition exists. The actuator resides on the last track accessed.
4. Read/Write/Seek mode is defined as when data is being read from or written to the disk. It is computed based on 40% seeking, 30% on-track read, and 30% on-track write.
5. Maximum seeking is defined as continuous random seek operations with minimum controller delay.
6. Standby mode is defined as when the motor is stopped, the actuator is parked, and all electronics except the interface control are in the sleep state. Standby occurs after a programmable timeout after the last host access. Drive ready and seek complete status exist. The drive leaves standby upon receipt of a command that requires disk access or upon receiving a spinup command.
7. Sleep is defined as when the spindle and actuator motors are off and the heads are latched in the landing zone. Receipt of a reset causes the drive to transition from the sleep to the standby mode.
8. Read/Write On Track is defined as 50% read operations and 50% write operations on a single physical track.

4.6 ACOUSTICS

Table 4-6 and Table 4-7 specify the acoustical characteristics of the Lightning 365/540/730AT hard disk drive.

Table 4-6 *Acoustical Characteristics—Sound Pressure*

OPERATING MODE	MEASURED NOISE (SOUND PRESSURE)	DISTANCE
Idle On Track	33 dBA (typical) 36 dBA (maximum)	39.3 in (1 m)

Table 4-7 *Acoustical Characteristics—Sound Power*

OPERATING MODE	MEASURED NOISE (SOUND POWER PER ISO 7779)
Idle On Track	4.0 Bels (typical) 4.2 Bels (maximum)

4.7 MECHANICAL DIMENSIONS

Height: 1.0 in.	(25.4 mm)
Width: 4.0 in.	(101.6 mm)
Depth: 5.75 in.	(146.1 mm)

Note: All dimensions are exclusive of any optional faceplate.

4.8 ENVIRONMENTAL CONDITIONS

Table 4-8 summarizes the environmental specifications of the Lightning 365/540/730AT hard disk drive.

Table 4-8 *Environmental Specifications*

PARAMETER	OPERATING	NONOPERATING
Temperature	0° to 55°C 32° to 131°F	–40° to 65°C –40° to 149°F
Temperature Gradient	24°C/hr maximum	48°C/hr maximum
Humidity[1] Maximum Wet Bulb	5% to 85% rh 40°C (104°F)	5% to 95% rh 46°C (115°F)
Humidity Gradient	30%/hr	30%/hr
Altitude[2]	–200 m to 3 km (–650 to 10,000 ft.)	–200 m to 12 km (–650 to 40,000 ft.)
Altitude Gradient	1.5 kPa/min	8 kPa/min

1. No condensation.
2. Altitude is relative to sea level.

4.9 SHOCK AND VIBRATION

The Lightning 365/540/730AT hard disk drive can withstand levels of shock and vibration applied to any of its three mutually perpendicular axes, or principal base axes, as specified in Table 4-9. A functioning drive can be subjected to specified *operating* levels of shock and vibration. When a drive has been subjected to specified *nonoperating* levels of shock and vibration, with power to the drive off, there will be no change in performance at power on.

When packed in its 1-pack shipping container, the Lightning 365/540/730AT drive can withstand a drop from 30 inches onto a concrete surface on any of its surfaces, six edges, or three corners. The 12-pack shipping container can withstand a drop from 30 inches onto a concrete surface on any of its surfaces, six edges, or three corners.

Table 4-9 *Shock and Vibration Specifications*

	OPERATING	**NONOPERATING**
Shock:		
1/2 sine wave, 11 ms duration (10 hits maximum)	6 G (no soft errors) 10 G (no unrecovered errors)	60 G (no damage)
1/2 sine wave, 3 ms duration (10 hits maximum)	18 G (no unrecovered errors)	
Vibration:		
Sine wave (peak to peak) 1.0 octave/minute sweep	1.0 Gpp 5–300 Hz 0.5 Gpp 300–500 Hz (no unrecovered errors)	2.0 Gpp 5–500 Hz (no damage)

4.10 RELIABILITY

Mean Time Between Failures (MTBF):	The projected field MTBF is 300,000 hours (150,000 Power On Hours (POH), typical usage). The Quantum MTBF numbers represent Bell-Core TR-TSY-000332 MTBF predictions and represent the minimum MTBF that Quantum or a customer would expect from the drive.
Component Life:	5 years
Preventive Maintenance (PM):	Not required
Start/Stop:	20,000 cycles (minimum)

4.11 DISK ERRORS

Table 4-10 provides the error rates for the Lightning 365/540/730AT hard disk drive.

Table 4-10 *Error Rates*

ERROR TYPE	MAXIMUM NUMBER OF ERRORS
Unrecovered read errors[1]	1 error per 10^{14} bits read
Transferred errors[2]	1.123 errors per 10^{24} bits read
Seek Errors[3]	1 error per 10^{6} seeks

1. Unrecovered read errors are errors that are not correctable using ECC or retries. The drive terminates retry reads either when a repeating error pattern occurs, or after eight unsuccessful retries and the application of double-burst error correction.
2. Transferred errors are those errors that are not detected nor subsequently corrected by the drive. These are the types of errors that the make a real difference to the user.
3. Seek errors occur when the actuator fails to reach (or remain) over the requested cylinder.

Chapter 5
BASIC PRINCIPLES OF OPERATION

This chapter describes the operation of Lightning 365/540/730AT functional subsystems. It is intended as a guide to the operation of the drive, rather than a detailed theory of operation.

5.1 LIGHTNING DRIVE MECHANISM

This section describes the drive mechanism. Section 5.2 describes the drive electronics. The Lightning 365/540/730AT hard disk drive consists of a mechanical assembly and a PCB as shown in Figure 5-1. The drawing is illustrated with two disks, showing the Lightning 540AT configuration. The Lightning 365AT hard disk drive contains only one hard disk.

The head/disk assembly (HDA) contains the mechanical subassemblies of the drive, which are sealed under a metal cover. The HDA consists of the following components:

- Base casting
- DC motor assembly
- Disk stack assembly
- Headstack assembly
- Rotary positioner assembly
- Automatic actuator lock
- Air filter

The drive is assembled in a Class-100 clean room.

CAUTION: To ensure that the air in the HDA remains free of contamination, never remove or adjust its cover and seals. Tampering with the HDA will void your warranty.

The Lightning 365/540/730AT is a one or two disk product family. The Lightning 365AT hard disk drive contains one magnetic disk and two read/write heads. The Lightning 540AT contains two magnetic disks and three read/write heads. The Lightning 730AT contains two magnetic disks and four read/write heads

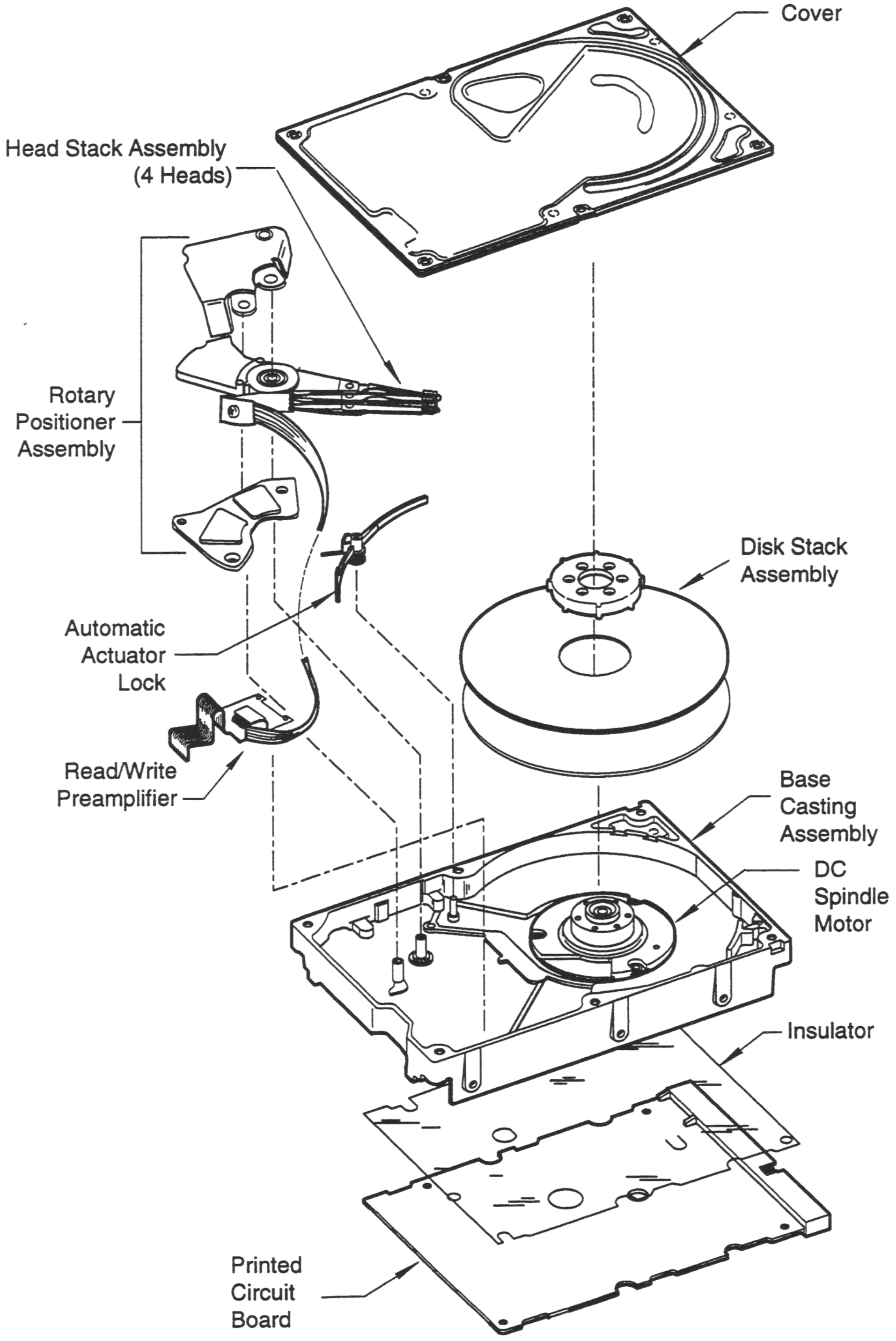

Figure 5-1 *Lightning 730AT Exploded View*

5.1.1 Base Casting Assembly

A single-piece, aluminum-alloy base casting provides a mounting surface for the drive mechanism and PCB. The base casting also acts as the flange for the DC motor assembly. To provide a contamination-free environment for the HDA, a gasket provides a seal between the base casting and the metal cover that encloses the drive mechanism.

5.1.2 DC Motor Assembly

Integral with the base casting, the DC motor assembly is a fixed-shaft, brushless DC spindle motor that drives the counter-clockwise rotation of the disks.

5.1.3 Disk Stack Assemblies

The disk stack assembly in the Lightning 365AT hard disk drive consists of one disk secured by a disk clamp. The Lightning 540/730AT hard disk drives contains two disks. The aluminum-alloy disks have a sputtered thin-film magnetic coating.

A carbon overcoat lubricates the disk surface, to prevent head and media wear due to head contact with the disk surface during head takeoff and landing. Head contact with the disk surface occurs only in the landing zone outside of the data area, when the disk is not rotating at full speed. The landing zone is located at the inner diameter of the disk, beyond the last cylinder of the data area.

The Lightning 365/540/730AT hard disk drive has 3,663 tracks per recording surface. Of these tracks, 5 are used for system data, leaving 3,658 for data. The data tracks are divided into 15 recording zones. The drive uses multiple zone recording, where each data track contains between 64 and 128 sectors, depending on the recording zone. The sectors per track allocation for each zone is provided in Table 5-1.

Table 5-1 *Cylinder Contents*

CYLINDER CONTENTS	ZONE[1]	NUMBER OF TRACKS	SECTORS PER TRACK	DATA RATE (Mbit/s)
System Data	0	5	100	
User Data	1	480	128	47.24
	2	266	126	46.48
	3	258	119	44.19
	4	227	114	42.44
	5	244	109	40.57
	6	198	105	38.86
	7	237	100	37.37
	8	250	93	34.78
	9	216	89	33.52
	10	235	85	31.24
	11	271	80	30.48
	12	239	75	28.54
	13	204	70	27.04
	14	250	63	24.47
	15	83	61	23.74

1. For user data, zone 15 is the innermost zone and zone 1 is the outermost zone.

5.1.4 Headstack Assembly

The headstack assembly consists of read/write heads, an E-block and coil joined together by insertion molding to form an E-block/coil subassembly, bearings, and a flex circuit. Read/write heads mounted to spring-steel flexures are swage mounted onto the rotary positioner assembly arms. The E-block is a single piece, die-cast design.

The flex circuit exits the HDA between the base casting and the cover. A cover gasket seals the gap. The flex circuit connects the headstack assembly to the PCB. The flex circuit contains a read preamplifier/write driver IC.

5.1.5 Rotary Positioner Assembly

The rotary positioner, or rotary voice-coil actuator, is a Quantum-proprietary design that consists of upper and lower permanent magnet plates bolted to the base casting, a rotary single-phase coil molded around the headstack mounting hub, and a bearing shaft. The magnets consist of two alternating poles bonded to the magnet plates. Resilient crash stops mounted on the magnet plates prevent the heads from being driven into the spindle or off the disk surface

Current from the power amplifier induces a magnetic field in the voice coil. Fluctuations in the field around the permanent magnets cause the voice coil to move. The movement of the voice coil positions the heads over the requested cylinder.

5.1.6 Automatic Actuator Lock

To ensure data integrity and prevent damage during shipment, the drive uses a dedicated landing zone and Quantum's patented Airlock®. The Airlock holds the headstack in the landing zone whenever the disks are not rotating. It consists of an air vane mounted near the perimeter of the disk stack and a locking arm that restrains the actuator arm assembly.

When DC power is applied to the motor and the disk stack rotates, the rotation generates an airflow on the surface of the disk. As the flow of air across the air vane increases with disk rotation, the locking arm pivots away from the actuator arm, enabling the headstack to move out of the landing zone. When DC power is removed from the motor, an electronic return mechanism automatically pulls the actuator into the landing zone, where the Airlock holds it in place.

5.1.7 Air Filtration

The Lightning 365/540/730AT hard disk drives are Winchester-type drives. The heads fly very close to the media surface. Therefore, it is essential that the air circulating within the drive be kept free of particles. Quantum assembles the drive in a Class-100, purified air environment, then seals the drive with a metal cover. When the drive is in use, the rotation of the disks forces the air inside of the drive through an internal filter.

The highest air pressure within the HDA is at the outer perimeter of the disks. A constant stream of air flows through a 0.3-micron circulation filter positioned in the base casting. As illustrated in Figure 5-2, air flows through the circulation filter in the direction of disk rotation. This design provides a continuous flow of filtered air when the disks rotate.

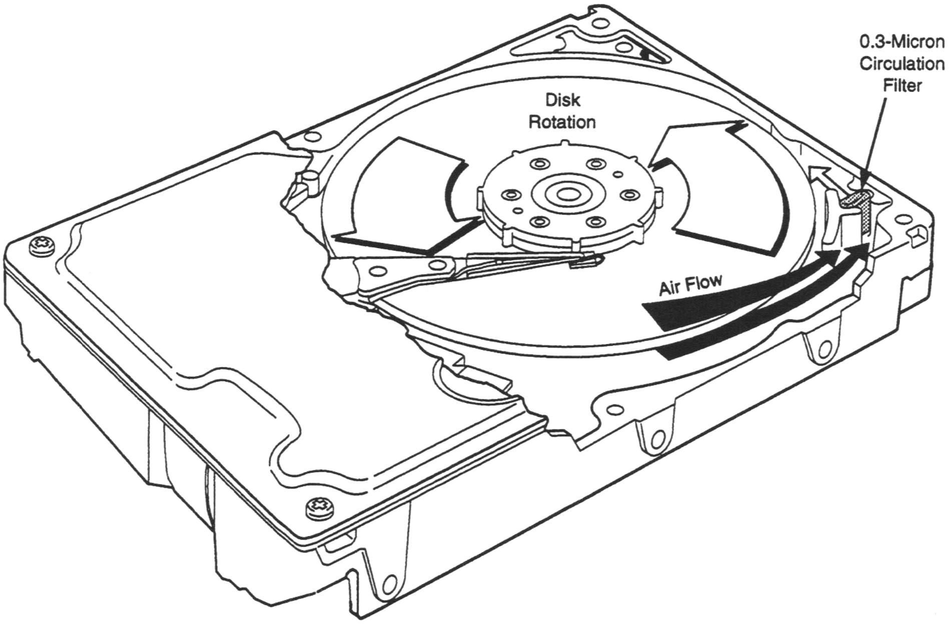

Figure 5-2 *HDA Air Filtration*

5.2 DRIVE ELECTRONICS

Advanced circuit design and the use of miniature surface-mounted devices and proprietary VLSI components enable the drive electronics, including the IDE bus interface, to reside on a single printed circuit board assembly (PCBA).

Note: The components are mounted on only one side of the PCB.

Figure 5-3 contains a simplified block diagram of the Lightning 365/540/730AT electronics.

The only electrical component not on the PCBA is the PreAmplifier and Write Driver IC. It is on the flex circuit (inside of the sealed HDA). Mounting the preamplifier as close as possible to the read/write heads improves the signal-to-noise ratio. The flex circuit (including the PreAmplifier and Write Driver IC) provides the electrical connection between the PCB, the rotary positioner assembly, and read/write heads.

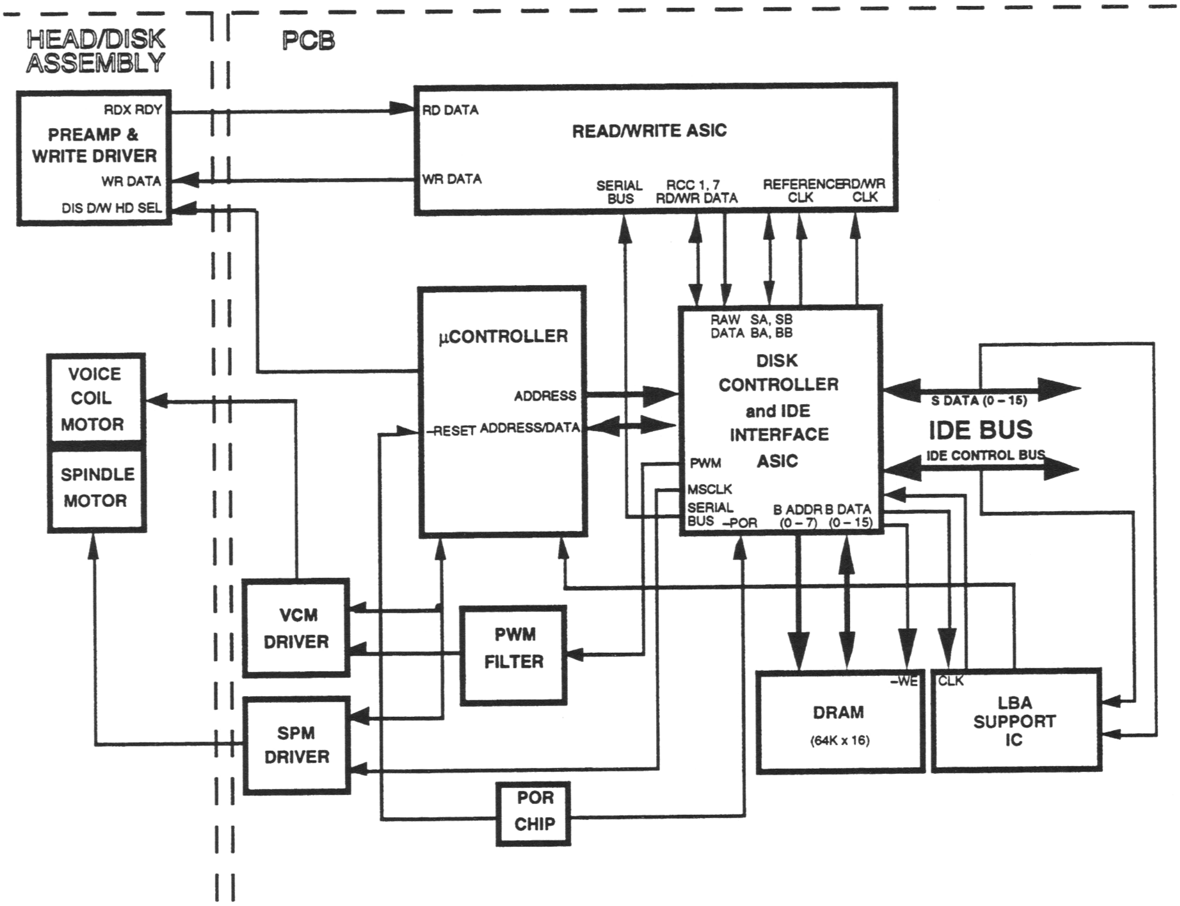

Figure 5-3 *Lightning 365/540/730AT Block Diagram*

5.2.1 µController

The µController provides local processor services to the drive electronics, under program control. The µController manages the resources of the Disk Controller and IDE Interface ASIC (DCIIA), the Read/Write ASIC, and the Actuator Driver. In addition, it controls the head selection process.

An internal 32Kbyte ROM contained within the µController provides program code that the µController executes to complete a drive spinup and recalibration procedure, after which the µController reads additional control code from the disk (diskware) and stores it in the buffer DRAM.

5.2.2 DCIIA

The DCIIA (Disk Controller and IDE Interface ASIC) shown in Figure 5-4 provides control functions to the drive under the direction of the µController.

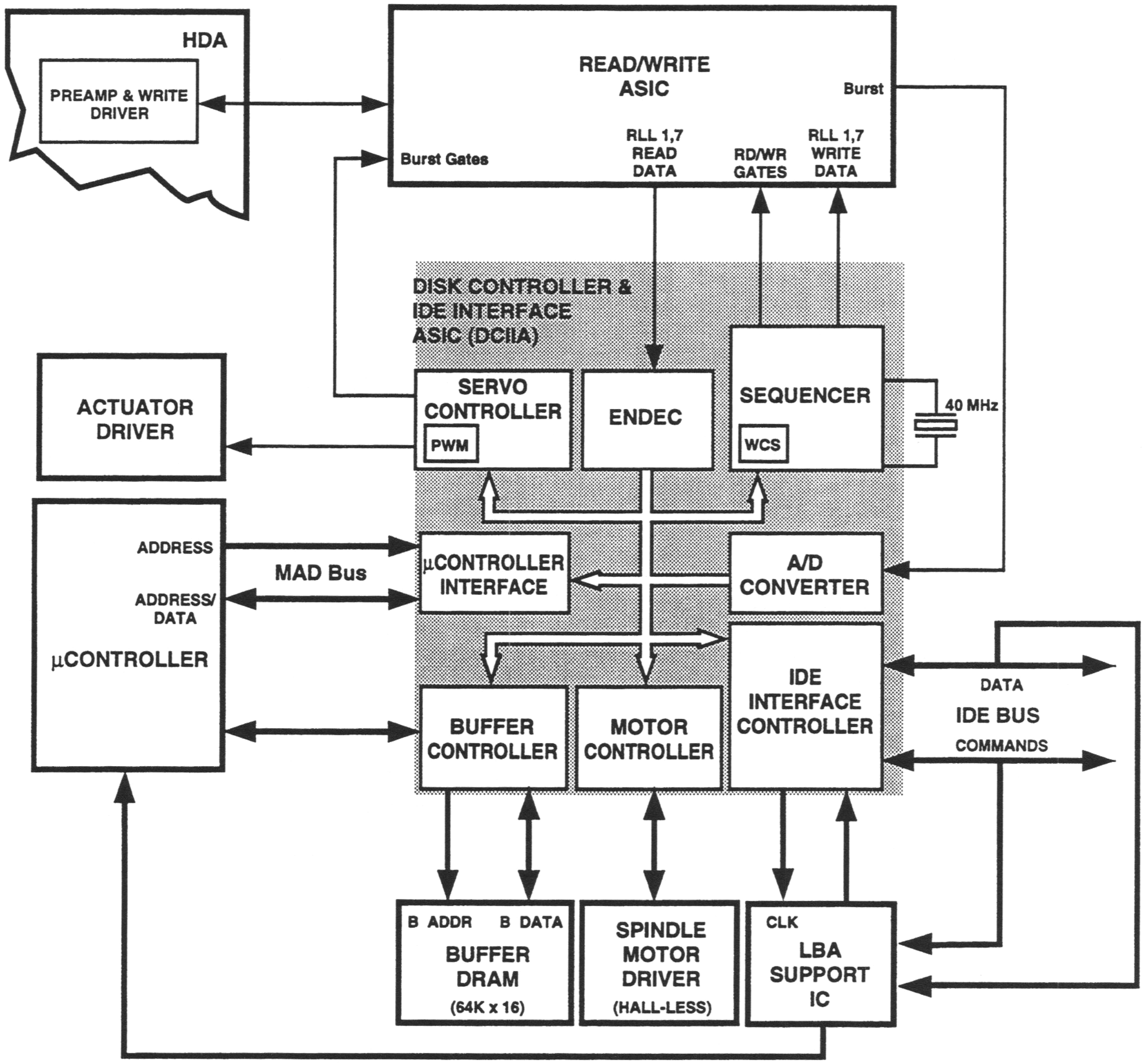

Figure 5-4 *DCIIA Block Diagram*

The DCIIA is a proprietary ASIC developed by Quantum. The DCIIA comprises eight functional modules (described below):

- 5-channel, 8-bit A/D Converter
- Encoder-Decoder (ENDEC)
- Sequencer
- Buffer Controller
- µController Interface
- Servo Controller, including PWM
- Motor Controller
- IDE Interface Controller

5.2.2.1 A/D Converter

The Analog to Digital converter (A/D) receives multiple burst analog inputs from the Read/Write ASIC. The A/D is used to sample the demodulated position information (burst inputs) and convert it to a digital signal the Servo Controller uses to position the HDA actuator.

5.2.2.2 Encoder/Decoder (ENDEC)

The ENDEC is a 1,7 RLL (Run Length Limited) encoder/decoder. The ENDEC encodes and decodes data under the control of the sequencer portion of the DCIIA. The ENDEC encodes write data and decodes read data. Write data is sent to the Sequencer for transfer to the Read/Write ASIC. Read data is input directly to the ENDEC from the Read/Write ASIC.

5.2.2.3 Sequencer

The sequencer controls the operation of the read and write channel portions of the DCIIA, including the ENDEC, using commands loaded into a 28 x 24-bit writable control store (WCS) by the µController. Each command word is 28 bits in length. To initiate a disk operation, the µController loads a set of these 28-bit commands into the WCS. Up to 24 commands may be loaded. Loading and manipulating the WCS is done through the µController Interface registers.

The sequencer also directly drives the read and write gates (RG, WG) of the Read/Write ASIC and the R/W PreAmplifier, as well as passing write data to the Precompensator circuit in the Read/Write ASIC. The sequencer handles the appending and processing of the ECC bytes for the read/write data, using a 112-bit, interleaved Reed-Solomon scheme with two cross-check bytes.

5.2.2.4 Buffer Controller

The buffer controller supports a 128Kbyte buffer, which is organized as 64K x 16 bits. The 16-bit width implementation provides a 20 MB/s maximum buffer bandwidth, which allows 6 MB/s disk channel operation with a minimum 6 MB/s host channel bandwidth. This increased bandwidth allows the µController to have direct access to the buffer, eliminating the need for a separate µController IC.

The buffer controller supports both drive and host address rollover and reloading, to allow for buffer segmentation. Drive and host addresses may be separately loaded for auto-write functions. A separate access channel is provided for the µController, allowing it to directly access the buffer.

The Buffer Controller operates under the direction of the µController.

5.2.2.5 µController Interface

The µController Interface provides the means for the µController to read and write data to the DCIIA modules to control their operation or supply them with needed information. It consists of both physical and logical components.

The physical component of the interface comprises the eight-bit MAD bus, eight address lines, a read strobe, a write strobe, an address latch enable signal, and a wait control line.

The logical component of the interface comprises internal control and data registers accessible to the µController. By writing and reading these registers, the µController loads the Sequencer, controls and configures the Buffer and Motor controllers, and passes coded servo information to the Servo Controller.

5.2.2.6 Servo Controller

The Servo Controller contains a 10-bit Digital to Analog converter (D/A), in the form of a Pulse Width Modulator (PWM). The PWM signal is output to the Actuator Driver to control the motion of the actuator. The Servo Controller also decodes raw data from the disk to extract the current position information. The position information is read by the µController and is used to generate the actuator control signal that is sent to the PWM. The actuator driver is an analog power amplifier circuit external to the DCIIA. The Servo Controller operates under the direction of the µController.

5.2.2.7 Motor Controller

The Motor Controller provides a reference clock for speed control of the hall-less Spindle Motor Driver. The Spindle Motor Driver is an analog power amplifier circuit external to the DCIIA.

5.2.2.8 IDE Interface Controller

The IDE Interface Controller portion of the DCIIA provides data handling, bus control, and transfer management services for the IDE interface. Configuration and control of the interface is accomplished by the µController across the MAD bus. Data transfer operations are controlled by the DCIIA Buffer Controller module.

5.2.3 Read/Write ASIC

The Read/Write ASIC shown in Figure 5-5 provides write data precompensation and read channel processing functions for the drive. The Read/Write ASIC receives the RD GATE signal, write pre-compensation control, reference oscillator, serial programming, and servo burst and sample gates from the DCIIA. The Read/Write ASIC sends encoded read data and the read reference clock, and receives write data from the DCIIA.

The Read/Write ASIC comprises six functional modules (described below):

- Pre-Compensator
- Programmable Filter
- Time Base Generator
- Pulse Detector
- Peak Detector and Servo Demodulator
- Data Synchronizer

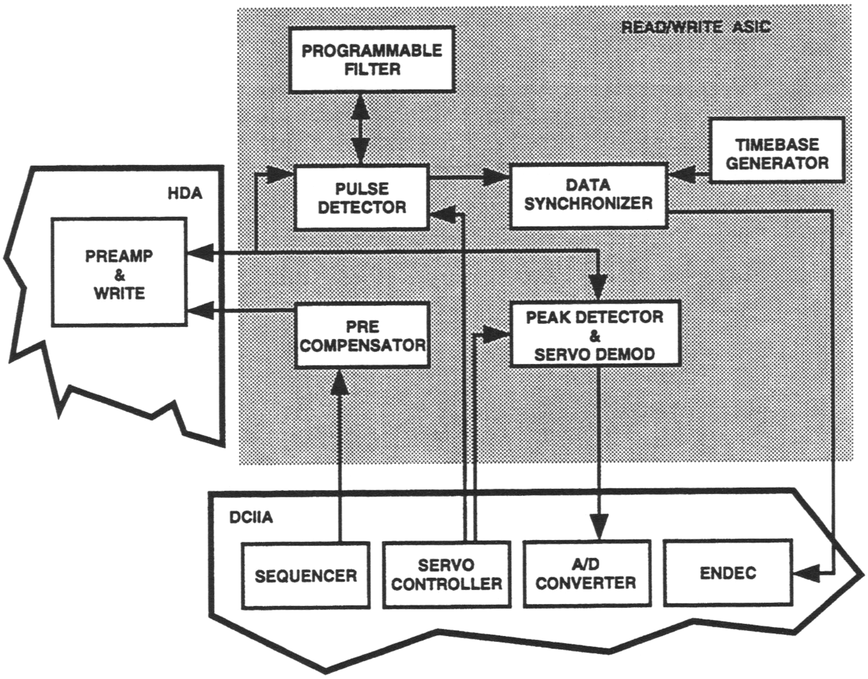

Figure 5-5 *Read/Write ASIC Block Diagram*

5.2.3.1 Pre-Compensator

The pre-compensator introduces pre-compensation to the write data received from the sequencer module in the DCIIA. The pre-compensated data is then passed to the R/W Pre-Amplifier and written to the disk. Pre-compensation reduces the intersymbol interference found in the read mode.

5.2.3.2 Programmable Filter

The DCIIA programs the Pulse Detector filter by writing data to it over the serial interface for each zone and head on the disk.

5.2.3.3 Timebase Generator

The frequency synthesizer in the timebase generator provides the reference frequency for the Data Synchronizer and the DCIIA. The µController programs the Timebase Generator with the appropriate frequency for each zone on the disk by writing data over the serial interface.

5.2.3.4 Pulse Detector

The pulse detector filters, amplifies, and differentiates the read data received from the R/W Pre-Amp. The read data at this point is 1,7 RLL encoded analog signals. Once converted to an asynchronous digital data stream, the read data is passed to the Data Synchronizer module for synchronization.

5.2.3.5 Peak Detector

The peak detector extracts the servo wedge Burst A, Burst B, and Burst C amplitude information from the read data signal. The gate inputs to the peak detector are sent from the Servo Controller module in the DCIIA. The gate inputs are used to sample the burst field amplitudes in the servo wedge.

5.2.3.6 Data Synchronizer

Using a phase-lock-loop (PLL), the Data Synchronizer synchronizes the read data to the read clock (after the correct address mark is recovered) and passes both to the ENDEC module in the DCIIA. The synthesizer generates the reference frequency to the PLL for data clock recovery and resynchronization.

5.2.4 PreAmplifier and Write Driver

The PreAmplifier and Write Driver provides write driver and read pre-amplifier functions, and R/W head selection. The write driver receives precompensated write data from the PreCompensator module in the Read/Write ASIC. The write driver then sends this data to the heads in the form of a corresponding alternating current. The read pre-amplifier amplifies the low-amplitude differential voltages generated by the R/W heads and transmits them to the Pulse Detector module in the Read/Write ASIC. Head select is determined by the µController.

5.3 SERVO SYSTEM

5.3.1 General Description

The servo system controls the positioning of the read/write heads and holds the read/write heads on track during read/write operations. The servo system also compensates for thermal offsets between heads on different surfaces, and any shock and vibration the drive is subjected to.

The Lightning 365/540/730AT uses a sectored servo system. Positioning information is radially encoded in 70 evenly-spaced servo bursts on each track. These servo burst wedges provide radial position information for each data head, 70 times per revolution. Because the drive uses multiple zone recording, where each zone has a different bit density, split data fields are necessary to optimally utilize the non-servo area of the disk. The split data fields are achieved by special processing through the DCIIA, and their presence is transparent to the host system. The servo area remains phase coherent across the surface of the disk, even though the disk is divided into various data zones. The main advantage of the sectored servo systems is that the data heads are also servo heads, which means that sectored servo systems eliminate the problems of static and dynamic offsets between heads on different surfaces.

The Lightning 365/540/730AT servo system is also classified as a digital servo because track following compensation is done in firmware. The bump detect, on-track, velocity profiles, and other “housekeeping” tasks are also done in firmware.

The servo system has three basic modes of operation (1) velocity mode, (2) settle mode, and (3) track following mode.

1. Velocity mode. The acceleration and deceleration of the actuator for seek lengths of 20 or more tracks is accomplished with a velocity loop. The velocity profile is calculated as the seek is in progress, using programmable coefficients. The bandwidth of the velocity loop is kept low, and feed forward is heavily used.

2. Settle mode.The settle mode is used for all accesses—head switches, 1- to 20-track seeks, and the end of all velocity seeks. The settle mode is a position loop with velocity damping. No feed forward is used for the settle mode.

3. Track following mode. The track following mode is used when “on-track.” This is also a position loop, with an integrator in the compensation.

5.3.2 Servo Burst and Track Information

Positional information is encoded on all tracks on all data surfaces. All data heads are also servo heads. The areas with servo/position information are called wedge areas. These wedge areas are evenly spaced radially around the disk, like spokes on a wheel. There are 70 wedge areas per track. Since the disk rotation is 75.0 revolutions/second, the position information is updated at 5250 Hz (70 x 75.0). This is also known as the sampling frequency *fs*. The sample period, Ts, is 1/*fs* = 190 µs. Every wedge area consists of four separate fields: (1) Automatic Gain Control (AGC)/ Sync field, (2) Sector Address Mark (SAM) field, (3) Track number and (4) Burst area. Since a Phase Lock Loop (PLL) is not used in the servo wedge area, time discrimination is used. Timing for all four fields is generated from the same crystal reference. This clock has a period of 25 nanoseconds, and will be referred to as T_{clk}. Data is encoded in the following manner: a servo data bit 1 = 1 0 0 1 0 0 0 0 0, and a servo data bit 0 = 1 0 0 0 0 0 1 0 0, with each digit having a T_{clk} width.

1. The AGC/sync field consists of a $3T_{clk}$ pattern, and is used by the AGC to acquire the proper amplitude for the encoded track number and position bursts. It is also used by the DCIIA Servo Controller for synchronizing to the raw data pulses. The total length of the AGC/sync field is $45T_{clk}$.
2. The SAM follows the sync field. It consists of a $14T_{clk}$ pattern repeated twice, followed by a servo data bit 0. Following the servo data bit 0 is either a servo data bit 0 or 1: this is also known as the index bit. If a one is decoded, then an index pulse is generated. The total length of the SAM field is $46T_{clk}$.
3. Following the index bit is the track number. The track number is a 12-bit, Gray-coded number. The Gray code to binary conversion is done in the DCIIA Servo Controller. Each Gray code bit is encoded as servo data bits. The total length of the track number is $108T_{clk}$.
4. Following the track number is the burst area. There are three bursts per servo wedge time, an A burst followed by the B burst and finally the C burst. When "on-track", the A and C burst will be at half amplitude. For even tracks the B burst will be full amplitude, and for odd tracks the B burst will be zero.

   The A, B, and C bursts are $42T_{clk}$ long. There are dc erase areas of $9T_{clk}$ before and after the burst fields, giving a total time of $144T_{clk}$ for the burst area.

5.3.3 Position and Velocity

The state of the servo system determines how the position information is derived. During the velocity and coarse settle modes of operation, the position signal is the convolution of the track number and A or B burst values and has a 1/256 of a track pitch resolution—about 0.4%. During track following and fine settle, the A and C bursts are used for the position information, and the resolution is at least 1/512th of a track pitch—about 0.2%. The velocity is the combination of two components: the difference between the present and last track, and a value that is proportional to the current.

5.4 READ AND WRITE OPERATIONS

The following paragraphs provide descriptions of the read channel, write channel, and IDE interface control operations.

5.4.1 The Read Channel

The drive has one read/write head for each data surface (two for the Lightning 365AT, three for the Lightning 540AT, and four for the Lightning 730AT). The signal path for the read channel begins at the read/write heads. As the magnetic flux transitions recorded on a disk pass under a head, they generate low-amplitude, differential output voltages. These read signals pass from the read/write head to the flex circuit's read preamplifier, which amplifies the signal. To ensure a high signal to noise ratio, preamplification occurs on the flex circuit because of its proximity to the heads.

The flex circuit transmits the preamplified signal from the HDA to the drive PCB. On the PCB, the Read/Write ASIC's AGC, Filter, Pulse Detector, and Data Synchronizer modules further amplify, filter, and process the read signal to reduce ambiguities (for example, drop-ins, drop-outs, and peak shift). In addition, the Data Synchronizer converts the signal from the serial encoded head data to a synchronized data stream, with its accompanying clock. The Read/Write ASIC then sends the resynchronized data output to Quantum's proprietary Disk Controller and IDE Interface ASIC (DCIIA).

The DCIIA manages the flow of data between the Data Synchronizer on the Read/Write ASIC and its IDE Interface Controller. It also controls data access for the external RAM buffer. The DCIIA ENDEC decodes the RLL 1,7 format to provide a serial bit stream. This NRZ (Non-Return to Zero) serial data is converted to 8-bit bytes. The Sequencer module identifies the data as belonging to the target sector. Data is presented to the host in 16-bit words.

After a full sector is read, the DCIIA checks to see if the firmware needs to apply ECC on-the-fly or single or double-burst correction to the data. The buffer controller section of the DCIIA stores the data in the Cache and transmits the data to the IDE Interface Controller module, which transmits the data to the IDE bus.

5.4.2 The Write Channel

For the write channel, the signal path follows the reverse order of that for the read channel. The host presents 16-bit words of data, by means of the IDE bus, to the DCIIA IDE Interface Controller. The Buffer Controller section of the DCIIA stores the data in the cache. Because data can be presented to the drive at a rate that exceeds the rate at which the drive can write data to a disk, data is stored temporarily in the cache. Thus, the host can present data to the drive at a rate that is independent of the rate at which the drive can write data to the disk.

Upon correct identification of the target address, the data is shifted to the Sequencer where an error correcting code is generated and appended. The Sequencer then converts the bytes of data to a serial bit stream. The DCIIA ENDEC encodes the data in the RLL 1,7 format, generates a preamble field, inserts address marks, and transmits the data to the Read/Write ASIC where the data is precompensated to reduce intersymbol interference. The data is then transmitted to the Write Driver by means of the write data lines.

The drive's DCIIA switches the PreAmplifier and Write Driver IC to write mode and selects a head. Once the Write Driver receives a write gate signal, it transmits current reversals to the head, which induces magnetic transitions on the disk.

5.4.3 Interface Control

The interface with the host system is through a 40-pin IDE interface connector. The DCIIA IDE Interface Controller module implements the IDE bus interface logic. Operating under the drive's µprocessor control, the IDE Interface Controller receives and transmits bytes of data over the bus.

The DCIIA Buffer Controller writes data to or reads data from the Cache over 16 data lines. Under µController direction, the Buffer Controller controls the transfer of data and handles the addressing of the Cache for the DCIIA. The internal data transfer rate to and from the Cache is 20 MB/s. This high transfer rate allows the DCIIA to communicate over the IDE bus at a PIO data transfer rate of 6.0 MB/s without using IORDY, up to 11.1 MB/s with PIO using IORDY, or a DMA transfer rate of up to 13.3 MB/s while it simultaneously controls disk-to-RAM transfers and µcontroller access to control code stored in the buffer RAM.

5.5 FIRMWARE FEATURES

This section describes the following firmware features:

- Disk caching
- Track and cylinder skewing
- Error detection and correction
- Defect management

5.5.1 Disk Caching

The Lightning 365/540/730AT hard disk drive incorporates DisCache, a 96K disk cache, to enhance drive performance.This integrated Adaptive Caching feature can significantly improve system throughput. Read and write caching can be enabled or disabled by using the SET CONFIGURATION command.

5.5.1.1 Adaptive Caching

The cache buffer for the Lightning drives features adaptive segmentation for more efficient use of the buffer's RAM. With this feature, the buffer space used for read and write operations is dynamically allocated. The cache can be flexibly divided into several segments, under program control. Each segment contains one cache entry.

A cache entry consists of the requested read data plus its corresponding prefetch data. Adaptive segmentation allows the drive to make optimum use of the buffer, the amount of stored data can be increased.

5.5.1.2 Read Cache

DisCache anticipates host-system requests for data and stores that data for faster access. When the host requests a particular segment of data, the caching feature uses a prefetch strategy to “look ahead” and automatically store the subsequent data from the disk into high-speed RAM. If the host requests this subsequent data, the RAM is accessed rather than the disk.

Since typically 50 percent or more of all disk requests are sequential, there is a high probability that subsequent data requested will be in the cache. This cached data can be retrieved in microseconds rather than milliseconds. As a result, DisCache can provide substantial time savings during at least half of all disk requests. In these instances, DisCache could save most of the disk transaction time by eliminating the seek and rotational latency delays that dominate the typical disk transaction. For example, in a 1K data transfer, these delays make up to 90 percent of the elapsed time.

DisCache works by continuing to fill its cache memory with adjacent data after transferring data requested by the host. Unlike a noncaching controller, Quantum's disk controller continues a read operation after the requested data has been transferred to the host system. This read operation terminates after a programmed amount of subsequent data has been read into the cache segment.

The cache memory consists of a 128K DRAM buffer with 96K allocated to hold the data, which can be directly accessed by the host by means of the READ and WRITE commands. The memory functions as a group of segments (ring buffers) with rollover points at the end of each segment (buffer). The unit of data stored is the logical block (that is, a multiple of the 512-byte sector). Therefore, all accesses to the cache memory must be in multiples of the sector size.The following commands force emptying of the cache:

- RESET
- WRITE LONG
- READ LONG
- READ DEFECT LIST
- EXECUTE DRIVE DIAGNOSTIC
- FORMAT TRACK
- IDENTIFY DRIVE
- READ CONFIGURATION
- SET CONFIGURATION
- WRITE BUFFER
- SLEEP

5.5.1.3 Write Cache

When a write command is executed with write caching enabled, the drive stores the data to be written in a DRAM cache buffer and immediately sends a COMMAND COMPLETE message to the host before the data is actually written to the disk. The host is then free to move on to other tasks, such as preparing data for the next data transfer, without having to wait for the drive to seek to the appropriate track or rotate to the specified sector.

While the host is preparing data for the next transfer, the drive immediately writes the cached data to the disk, usually completing the operation in less than 20 ms after issuing COMMAND COMPLETE. With WriteCache, a single-block, random write, for example, requires only about 3 ms of host time. Without WriteCache, the same operation would occupy the host for about 20 ms.

WriteCache allows data to be transferred in a continuous flow to the drive rather than as individual blocks of data separated by disk access delays. This is achieved by taking advantage of the ability to write blocks of data sequentially on a disk that is formatted with a 1:1 interleave. This means that as the last byte of data is transferred out of the write cache and the head passes over the next sector of the disk, the first byte of the of the next block of data is ready to be transferred, thus there is no interruption or delay in the data transfer process.

The WriteCache algorithm fills the cache buffer with new data from the host while simultaneously transferring the data to the disk that the host previously stored in the cache.

5.5.1.4 Performance Benefits

In a drive without DisCache, there is a delay during sequential reads because of the rotational latency even if the disk actuator already is positioned at the desired cylinder. DisCache eliminates this rotational latency time (6.7 ms on average) when requested data resides in the cache.

Moreover, the disk must often service requests from multiple processes in a multitasking or multiuser environment. In these instances, while each process might request data sequentially, the disk drive must share time among all these processes. In most disk drives, the heads must move from one location to another. With DisCache, even if another process interrupts, the drive continues to access the data sequentially from its high-speed memory. In handling multiple processes, DisCache achieves its most impressive performance gains, saving both seek and latency time (23 ms on average) when desired data resides in the cache.

The Lightning 365/540/730AT hard disk drive uses a least-recently used segment-replacement strategy. Each time there is a cache hit on a segment or data on a segment is replaced, the segment is time stamped as the most recently used. On a data-transfer operation involving reading from the disk, the new data replaces the data in the least recently used cache segment.

The cache can be flexibly divided into several segments, under program control. Each segment contains one cache entry. A cache entry consists of the requested read data plus its corresponding prefetch data.

The requested read data takes up a certain amount of space in the cache segment so the corresponding prefetch data can essentially occupy the rest of the space within the segment. The other factors determining prefetch size are the maximum and minimum prefetch. The drive's prefetch algorithm dynamically controls the actual prefetch value based on the current demand, with the consideration of overhead to subsequent commands.

5.5.2 Track and Cylinder Skewing

Track and cylinder skewing in the Lightning 365/540/730AT minimizes latency time and thus increases data throughput.

5.5.2.1 Track Skewing

Track skewing reduces the latency time that results when the drive must switch read/write heads to access sequential data. A track skew is employed such that the next logical sector of data to be accessed will be under the read/write head once the head switch is made and the data is ready to be accessed. Thus, when sequential data is on the same cylinder but on a different disk surface, a head switch is needed but not a seek. Since the sequential head-switch time is well defined on the Lightning 365/540/730AT, the sector addresses can be optimally positioned across track boundaries to minimize the latency time during a head switch. See Table 5-2.

5.5.2.2 Cylinder Skewing

Cylinder skewing also is used to minimize the latency time associated with a single-cylinder seek. The next logical sector of data that crosses a cylinder boundary is positioned on the drive such that after a single-cylinder seek is performed, and when the drive is ready to continue accessing data, the sector to be accessed is positioned directly under the read/write head. Therefore, the cylinder skew takes place between the last sector of data on the last head of a cylinder and the first sector of data on the first head of the next cylinder. Since single-cylinder seeks are well defined on the Lightning 365/540/730AT, the sector addresses can be optimally positioned across cylinder boundaries to minimize the latency time associate with a single-cylinder seek. See Table 5-2.

Table 5-2 *Track and Cylinder Skews*

ZONE	SECTORS PER TRACK	µS PER SECTOR	ROUNDED TRACK SKEW (IN SECTORS)	NUMBER OF CYLINDERS	ROUNDED CYLINDER SKEW (IN SECTORS)
System (0)	100	117.60	31	5	38
1	128	92.47	39	480	49
2	126	93.98	38	266	47
3	119	98.84	37	258	46
4	114	102.92	35	227	43
5	109	107.67	33	244	41
6	105	112.41	32	198	40
7	100	116.89	30	237	38
8	93	125.58	28	250	35
9	89	130.30	27	216	34
10	85	139.83	25	235	32
11	80	143.33	25	271	31
12	75	153.02	23	239	29
13	70	161.53	22	204	27
14	63	178.50	20	250	25
15	61	183.99	20	83	25

5.5.3 Error Detection and Correction

As disk drive areal densities increase, obtaining extremely low error rates requires a new generation of sophisticated error correction codes. Quantum Lightning 365/540/730AT series hard disk drives implement 112-bit single- and double-burst Reed-Solomon error correction techniques to reduce the uncorrectable read error rate to less than one bit in 1 x 10^{14} bits read.

When errors occur, an automatic retry and a more rigorous double-burst correction algorithm enable the correction of any sector with two bursts of three incorrect bytes each or up to six multiple random one-byte burst errors. In addition to these advanced error correction capabilities, the drive uses an additional cross-checking code and algorithm, to double check the main ECC correction. This greatly reduces the probability of a miscorrection.

5.5.3.1 Background Information on Error Correction Code and ECC On-the-Fly

A sector for Lightning 365/540/730AT drives is comprised of 512 bytes of user data, followed by two cross-checking (XC) bytes (16 bits), followed by twelve ECC check bytes (96 bits). The two cross-checking bytes are used to double check the main ECC correction and reduce the probability of miscorrection. Single burst errors of up to 24 bits within one sector can be corrected "on-the-fly," in real time as they occur, allowing a high degree of data integrity with no impact to the drive's performance.

The drive does not need to re-read a sector on the next disk revolution or apply ECC for those errors that are corrected on-the-fly. Errors corrected in this manner are invisible to the host system.

When errors cannot be corrected on-the-fly, an automatic retry and a more rigorous double-burst error correction algorithm enable the correction of any sector with two bursts of three incorrect bytes each or up to 6 multiple random one-byte burst errors. In addition to this error correction capability, the drive's implementation of an additional cross-checking code and algorithm double checks the main ECC correction and greatly decreases the likelihood of miscorrection.

The twelve ECC check bytes shown in Figure 5-6 are used to detect and correct errors. The cross-checking and ECC data is computed and appended to the user data when the sector is first written.

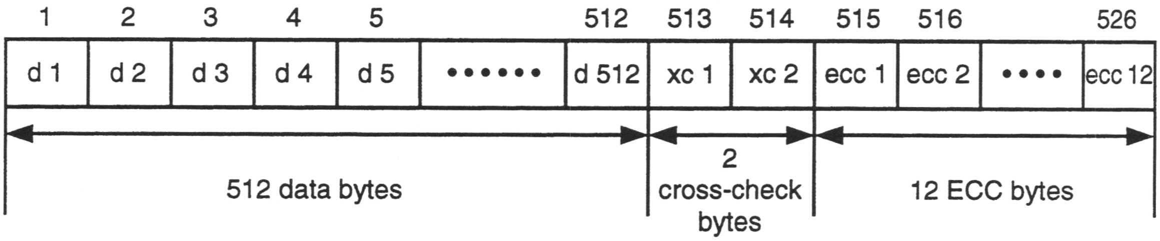

Figure 5-6 *Sector Data Field with ECC Check Bytes*

To obtain the ECC check byte values, each byte (including cross-checking and ECC bytes) within the sector is interleaved into one of three groups, where the first byte is in interleave 1, the second byte is in interleave 2, the third byte is in interleave 3, the fourth byte is in interleave 1, the fifth byte is in interleave 2, and so on, as shown in Figure 5-7.

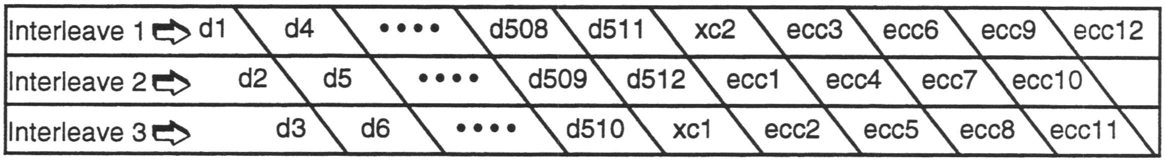

Figure 5-7 *Byte Interleaving*

Note: ECC interleaving is not the same as the sector interleaving that is done on the disk.

Each of the three interleaves is encoded with four ECC bytes, resulting in the twelve ECC bytes at the end of the sector. The two cross checking bytes are derived from all 512 data bytes. The combination of the interleaving and the nature of the ECC formulas enable the drive to know where the error occurs.

Because the ECC check bytes follow the cross checking bytes, errors found within the cross-checking bytes can be corrected. Due to the power and sophistication of the code, errors found within the ECC check bytes can also be corrected. Errors in the cross-check or ECC bytes can be corrected on-the-fly if their characteristics fall into the guidelines of a single-burst correctable error.

Each time a sector of data is read, Lightning 365/540/730AT drives will generate a new set of ECC check bytes and cross-checking bytes from the user data. These new check bytes are compared to the ones originally written to the disk. The difference between the newly computed and original check bytes is reflected in a set of twelve *syndromes* and two cross checking syndromes, which corresponds to the number of check bytes. If all of the syndrome values equal zero, the data was read with no errors, and the sector is transferred to the host system. If any of the syndromes do not equal zero, an error has occurred. The type of correction the drive applies depends on the nature and the extent of the error.

High speed on-the-fly error correction saves several milliseconds on each single-burst error, because there is no need to wait for a disk revolution to bring the sector under the head for re-reading.

Correction of Single-Burst Errors On-the-Fly

Single-burst errors may have up to three erroneous bytes (24 bits) within a sector, provided that each byte of the three must occur in a different interleave. In other words, if the first error bit is in interleave 1, the last error bit must occur no later than interleave 3. If the first error bit falls in interleave 1, and the last error bit falls in the next interleave 1, the error is uncorrectable on-the-fly. In Figure 5-8, the 24-bit error is correctable, because it is spread across three distinct interleaves. The 18-bit error is uncorrectable on-the-fly because it falls across four interleaves: two interleave 1s, interleave 2, and interleave 3.

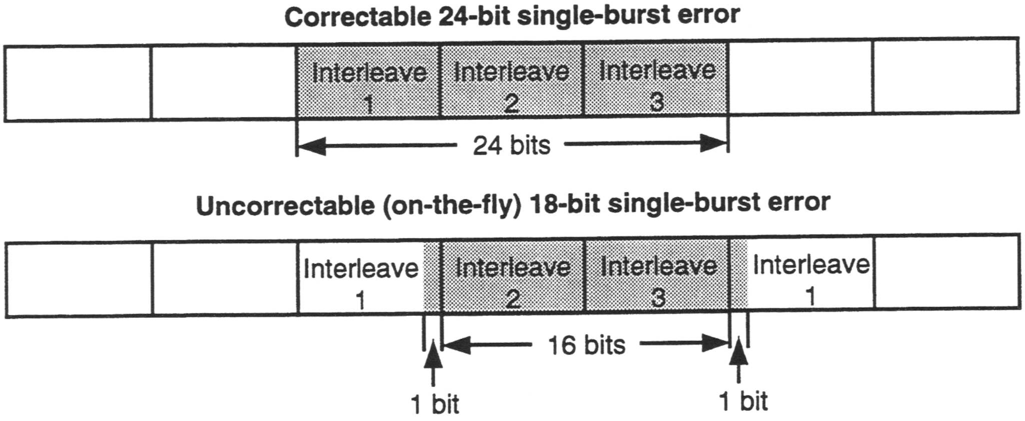

Figure 5-8 *Single-Burst Error Correctability*

Note: In Figure 5-8, the shaded portions represent data containing errors.

The 18-bit error can be corrected if the drive rereads the sector and applies double-burst error correction techniques. Any 17-bit error can always be corrected on-the-fly because each byte is guaranteed to occupy different interleaves.

Correction of Double-Burst Errors

Through sophisticated algorithms, Lightning 365/540/730AT Drives have the capability to correct double-burst errors, even though the probability of their occurrence is low. Double-burst errors can be simply viewed as two spans of errors within one sector. More specifically, correctable double-burst errors must have two or fewer erroneous bytes per interleave, and cannot be corrected on-the-fly.

The drive's Reed-Solomon ECC corrects double-burst errors up to 48 bits long, (provided that the error consists of two or fewer bytes residing in each of the interleaves).

If the double-burst correction is successful, the data from the sector can be written to a spare sector and the logical address will be mapped to the new physical location.

Double-Burst Error Examples

In the example shown in Figure 5-9 C, the 42-bit error is uncorrectable since it occupies more than two erroneous bytes per interleave.

The other two 48-bit errors, shown in Figure 5-9 A and B, are correctable because no more than two error bytes of the entire error reside in any one of the interleaves.

Note: Any 41-bit error burst can be corrected using double-burst error correction because no more than two bytes can occupy each interleave.

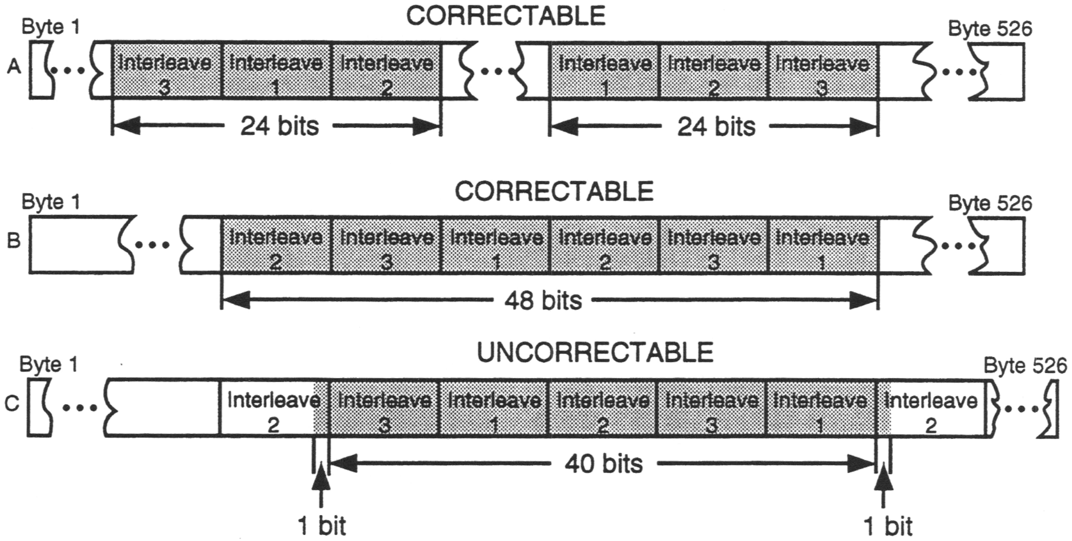

Figure 5-9 *Correctable and Uncorrectable Double-Burst Errors*

Multiple Random Burst Errors

The drive's ECC can correct up to 48 bits of multiple random errors, provided that the incorrect bytes follow the guidelines for correctable double-burst errors. Up to 24 bits of multiple random errors can be corrected on-the-fly if only one byte per interleave contains an error. If more than two bytes in any one interleave are in error, the sector cannot be corrected. Figure 5-10 shows an example of a correctable random burst error consisting of 6 bytes (48 bits). This random burst error is correctable because no more than two bytes within each interleave are in error.

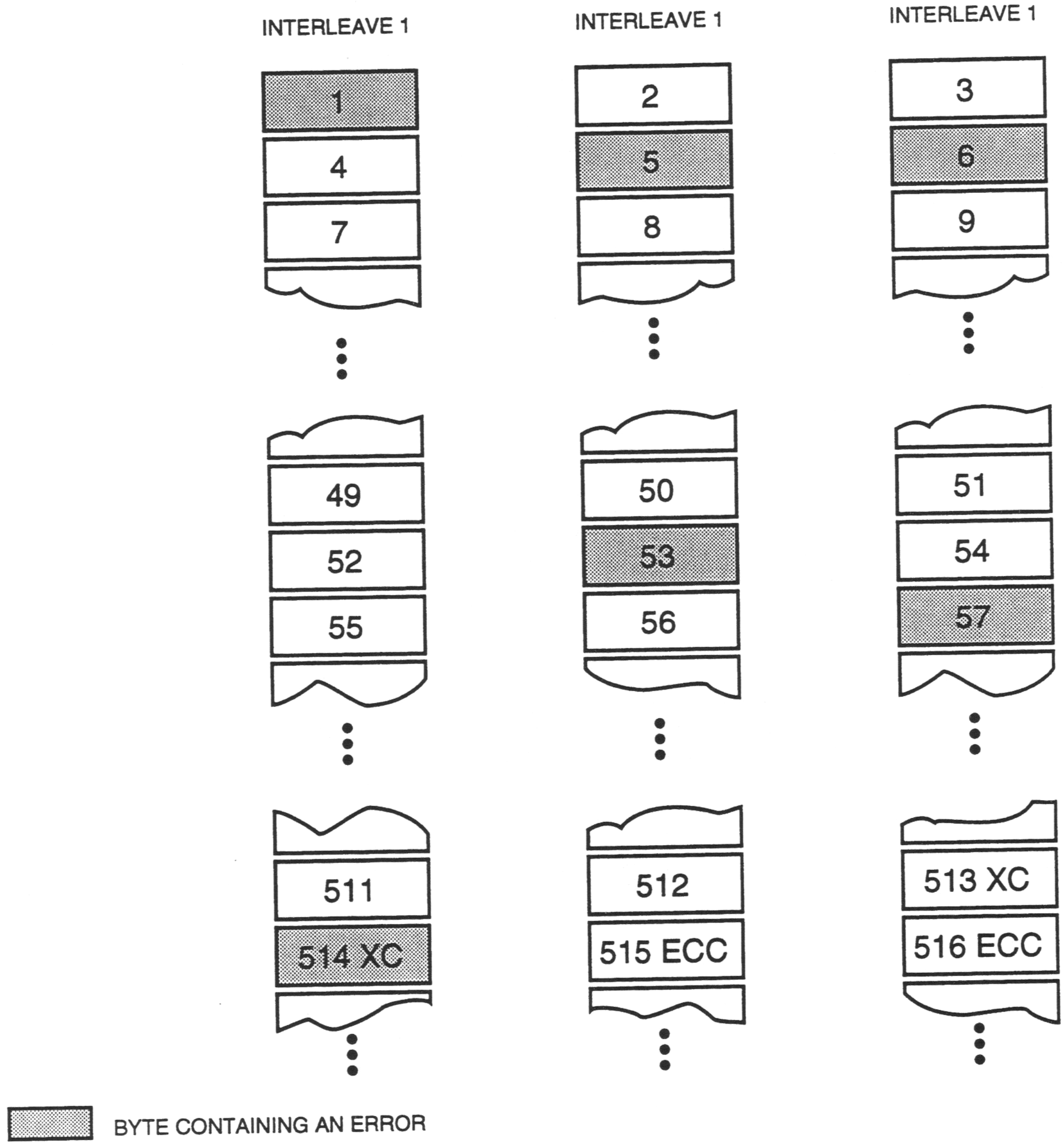

Figure 5-10 *Six Correctable Random Burst Errors*

5.5.3.2 ECC Error Handling

When a data error occurs, the Lightning 365/540/730AT hard disk drive checks to see if the error is correctable on-the-fly. This process takes about 200 µs. If the error is correctable on-the-fly, the error is corrected and the data is transferred to the host system.

If the data is not correctable on-the-fly, the sector is re-read in an attempt to read the data correctly without applying the double-burst ECC correction. Before invoking the complex double-burst ECC algorithm, the drive will always try to recover from an error by attempting to re-read the data correctly. This strategy prevents invoking correction on non-repeatable errors. Each time a sector in error is re-read a set of ECC syndromes is computed. If all of the syndrome values equal zero, the data was read with no errors, and the sector is transferred to the host system. If any of the syndrome values do not equal zero, an error has occurred, the syndrome values are retained, and another re-read is invoked.

Note: Non-repeatable errors are usually related to the signal to noise ratio of the system. They are not due to media defects.

When the sets of syndromes from two consecutive re-reads are the same, a stable syndrome has been achieved. This event may be significant depending on whether the automatic read reallocation or early correction features have been enabled. If the early correction feature has been enabled and a stable syndrome has been achieved, double-burst ECC correction is applied, and the appropriate message is transferred to the host system (e.g., corrected data, etc.).

Note: These features can be enabled or disabled through the ATA configuration command. The ECC bit enables early ECC double-burst correction if a stable syndrome has been achieved before all of the re-reads have been exhausted. The ARRE bit enables the automatic reallocation of defective sectors.

If the automatic read reallocation feature is enabled, the drive, when encountering double-burst errors, will attempt to re-read up to 8 times the retry count set in the AT configuration bytes. In this case, the ECC correction algorithm is divided into three parts.

Note: The Lightning 365/540/730AT is shipped from the factory with the automatic read reallocation feature enabled so that any new defective sectors can be easily and automatically reallocated for the average AT end user.

5.5.4 Defect Management

The Lightning 365AT and 540AT allocate one sector per cylinder as a spare, and the Lightning 730AT allocates two sectors per cylinder as spares. In the factory, the media is scanned for defects. If a sector on a cylinder is found to be defective, the address of the sector is added to the drive's defect list. Sectors located physically subsequent to the defective sector are assigned logical block addresses such that a sequential ordering of logical blocks is maintained. This inline sparing technique is employed in an attempt to eliminate slow data transfer that would result from a single defective sector on a cylinder.

If more than one sector is found defective on a cylinder, the inline sparing technique is applied to the first sector only. The remaining defective sectors are replaced with the nearest available spare sectors on nearby cylinders. Such an assignment of additional replacement sectors from nearby sectors rather than having a central pool of spare sectors is an attempt to minimize the motion of the actuator and head that otherwise would be needed to find a replacement sector. The result is minimal reduction of data throughput.

Defects that occur in the field are known as *grown* defects. If such a defective sector is found in the field, the sector is reallocated according to the same algorithm used at the factory for those sectors that are found defective *after* the first defective sector on a cylinder; that is, inline sparing is not performed on these grown defects. Instead, the sector is reallocated to an available spare sector on a nearby cylinder.

Sectors are considered to contain grown defects if the double-burst ECC algorithm must be applied to recover the data. If this algorithm is successful, the corrected data is stored in the newly allocated sector. If the algorithm is not successful, the erroneous data is stored in the newly allocated sector, and a flag is set in the data ID field that causes the drive to report an ECC error each time the sector is read. This condition remains until the sector is rewritten.

Chapter 6
IDE BUS INTERFACE AND ATA COMMANDS

This chapter describes the interface between Lightning 365/540/730AT hard disk drives and the IDE bus. The commands that are issued from the host to control the drive are listed, as well as the electrical and mechanical characteristics of the interface.

6.1 INTRODUCTION

Lightning 365/540/730AT hard disk drives use the standard IBM PC IDE bus interface, and are compatible with systems that provide an IDE interface connector on the motherboard. It may also be used with a third-party adapter board in systems that do not have a built-in IDE adapter. The adapter board plugs into a standard 16-bit expansion slot in an AT-compatible computer. A cable connects the drive to the adapter board.

6.2 SOFTWARE INTERFACE

Lightning 365/540/730AT drives are controlled by the Basic Input/Output System (BIOS) program residing in an IBM PC AT, or compatible PC. The BIOS communicates directly with the drive's built-in controller. It issues commands to the drive and receives status information from the drive.

6.3 MECHANICAL DESCRIPTION

6.3.1 Drive Cable and Connector

The hard disk drive connects to the host computer by means of a cable. This cable has a 40-pin connector that plugs into the drive, and a 40-pin connector that plugs into the host computer. At the host end, the cable plugs into either an adapter board residing in a host expansion slot or an on-board IDE adapter.

If two drives are connected by a cable with two 40-pin drive connectors, the cable-select feature of the Lightning 365/540/730AT automatically configures each as either drive 0 or drive 1 depending on the configuration of pin 28 on the connector. See Section 3.3.1, "Cable Select (CS) Jumper," for more information about the cable select jumper.

6.4 ELECTRICAL INTERFACE

6.4.1 IDE Bus Interface

A 40-pin IDE interface connector on the motherboard or an adapter board provides an interface between the drive and a host that uses an IBM PC AT bus. The IDE interface contains bus drivers and receivers compatible with the standard AT bus. The AT-bus interface signals D8–D15, INTRQ, and IOCS16– require the IDE adapter board to have an extended I/O-bus connector.

The IDE interface buffers data and control signals between the drive and the AT bus of the host system, and decodes addresses on the host address bus. The Command Block Registers on the drive accept commands from the host system BIOS.

Note: Some host systems do not read the Status Register after the drive issues an interrupt. In such cases, the interrupt may not be acknowledged. To overcome this problem, you may have to configure a jumper on the motherboard or adapter board to allow interrupts to be controlled by the drive's interrupt logic. Read your motherboard or adapter board manual carefully to find out how to do this.

6.4.1.1 Electrical Characteristics

All signals are transistor-transistor logic (TTL) compatible—with logic 1 greater than 2.0 volts and less than 5.25 volts; and logic 0 greater than 0.0 volts and less than 0.8 volts. Neither the adapter board, motherboard interface, or drives require terminating resistors.

6.4.1.2 Drive Signals

The drive connector (J1, section C) connects the drive to an adapter board or onboard IDE adapter in the host computer. J1, section C is a 40-pin shrouded connector with two rows of 20 pins on 100-mil centers. J1 has been keyed by removing pin 20. The connecting cable is a 40-conductor flat ribbon cable, with a maximum length of 18 inches.

describes the signals on the drive connector (J1, section C). The drive does not use all of the signals provided by the IDE bus. Table 6-2 shows the relationship between the drive connector (J1, section C) and the IDE bus.

Note: In , the following conventions apply:

A minus sign follows the name of any signal that is asserted as active low.
Direction (DIR) is in reference to the drive.
IN indicates input to the drive.
OUT indicates output from the drive.
I/O indicates that the signal is bidirectional.

Table 6-1 *Drive Connector Pin Assignments (J1, Section C)*

SIGNAL	NAME	DIR	PIN	DESCRIPTION
Reset	RESET–	IN	1	Drive reset signal from the host system, inverted on the adapter board or motherboard. Asserted for at least 300 ns during start up and deasserted thereafter, unless some event subsequently requires that the drive be reset. The RESET– signal does *not* alter the value of any drive parameters previously set, so it is not necessary to issue an INITIALIZE DRIVE PARAMETERS command after asserting RESET–.
Ground	Ground	—	2	Ground between the host system and the drive.
Data Bus		I/O	3–18	An 8/16-bit, bidirectional data bus between the host and the drive. D0–D7 are used for 8-bit transfers, such as registers and ECC bytes.
	DD0		17	Bit 0
	DD1		15	Bit 1
	DD2		13	Bit 2
	DD3		11	Bit 3
	DD4		9	Bit 4
	DD5		7	Bit 5
	DD6		5	Bit 6
	DD7		3	Bit 7
	DD8		4	Bit 8
	DD9		6	Bit 9
	DD10		8	Bit 10
	DD11		10	Bit 11
	DD12		12	Bit 12
	DD13		14	Bit 13
	DD14		16	Bit 14
	DD15		18	Bit 15
Ground	Ground	—	19	Ground between the host system and the drive.
Keypin	KEYPIN	—	20	Pin removed to key the interface connector.
DMA Request	DMARQ	OUT	21	Asserted by the drive when it is ready to exchange data with the host. The direction of the data transfer is determined by DIOW– and DIOR–. DMARQ is used in conjunction with DMACK–; that is, the drive waits until the host asserts DMACK– before deasserting DMARQ. DMARQ is then reasserted if there is additional data to transfer.
Ground	Ground	—	22	Ground between the host system and the drive.

Table 6-1 *Drive Connector Pin Assignments (J1, Section C) (Continued)*

SIGNAL	NAME	DIR	PIN	DESCRIPTION
I/O Write	DIOW–	IN	23	The rising edge of this write strobe provides a clock for data transfers from the host data bus (DD0–DD7 or DD0–DD15) to a register or to the drive's data port.
Ground	Ground	—	24	Ground between the host system and the drive.
I/O Read	DIOR–	IN	25	The rising edge of this read strobe provides a clock for data transfers from a register or the drive's data port to the host data bus (DD0–DD7 or DD0–DD15). The rising edge of DIOR– latches data at the host.
Ground	Ground	—	26	Ground between the host system and the drive.
I/O Channel Ready	IORDY	OUT	27	When the drive is not ready to respond to a data transfer request, the IORDY signal is asserted active low to extend the host transfer cycle of any host register read or write access. When IORDY is deasserted, it is in a high-impedance state and it is the host's responsibility to pull this signal up to a high level (if necessary).
Cable Select (Quantum specific)		—	28	This is a Quantum-specific signal from the host that allows the drive to be configured as drive 0 when the signal is 0 (grounded), and as drive 1 when the signal is 1 (high).
DMA Acknowledge	DACK1–	IN	29	Used by the host to respond to the drive's DMARQ signal. DMARQ signals that there is more data available for the host.
Ground	Ground	—	30	Ground between the host system and the drive.
Interrupt Request	INTRQ	OUT	31	An interrupt to the host system. Asserted only when the drive microprocessor has a pending interrupt, the drive is selected, and the host clears nIEN in the Device Control Register. When nIEN is a 1 or the drive is not selected, this output signal is in a high-impedance state, regardless of the presence or absence of a pending interrupt. INTRQ is deasserted by an assertion of RESET–, the setting of SRST in the Device Control Register, or when the host writes to the Command Register or reads the Status Register. When data is being transferred in programmed I/O (PIO) mode, INTRQ is asserted at the beginning of each data block transfer. Exception: INTRQ is not asserted at the beginning of the first data block transfer that occurs when any of the following commands executes: FORMAT TRACK, Write Sector, WRITE BUFFER, or WRITE LONG.

Table 6-1 *Drive Connector Pin Assignments (J1, Section C) (Continued)*

SIGNAL	NAME	DIR	PIN	DESCRIPTION
16-Bit I/O	IOCS16–	OUT	32	An open-collector output signal. Indicates to the host system that the 16-bit data port has been addressed and that the drive is ready to send or receive a 16-bit word. When transferring data in PIO mode, if IOCS16– is not asserted, D0–D7 are used for 8-bit transfers; if IOCS16– is asserted, D0–D15 are used for 16-bit data transfers.
Drive Address Bus				A 3-bit, binary-coded address supplied by the host when accessing a register or the drive's data port.
Bit 1	DA1	IN	33	
Bit 0	DA0	IN	35	
Bit 2	DA2	IN	36	
Passed Diagnostics	PDIAG–	I/O	34	Drive 0 (Master) monitors this Drive 1 (Slave) open-collector output signal, which indicates the result of a diagnostics command or reset. Each drive has a 10K pull-up resistor on this signal. Following the receipt of a power-on reset, software reset, or RESET– drive 1 negates PDIAG– within 1 ms. PDIAG– indicates to drive 0 that drive 1 is busy (BSY=1). Then, drive 1 asserts PDIAG– within 30 seconds, indicating that drive 1 is no longer busy (BSY=0) and can provide status information. Following the assertion of PDIAG–, drive 1 is unable to accept commands until drive 1 is ready (DRDY=1)—that is, until the reset procedure for drive 1 is complete. Following the receipt of a valid EXECUTE DRIVE DIAGNOSTIC command, drive 1 negates PDIAG– within 1 ms, indicating to drive 0 that it is busy and has not yet passed its internal diagnostics. If drive 1 is present, drive 0 waits for drive 1 to assert PDIAG– for up to 5 seconds after the receipt of a valid EXECUTE DRIVE DIAGNOSTIC command. Since PDIAG– indicates that drive 1 has passed its internal diagnostics and is ready to provide status, drive 1 clears BSY prior to asserting PDIAG–. If drive 1 fails to respond during reset initialization, drive 0 reports its own status after completing its internal diagnostics. Drive 0 is unable to accept commands until drive 0 is ready (DRDY=1)—that is, until the reset procedure for drive 0 is complete.

Table 6-1 *Drive Connector Pin Assignments (J1, Section C) (Continued)*

SIGNAL	NAME	DIR	PIN	DESCRIPTION
Chip Select 0	CS1FX–	IN	37	Chip-select signal decoded from the host address bus. Used to select the host-accessible Command Block Registers.
Chip Select 1	CS3FX–	IN	38	Chip select signal decoded from the host address bus. Used to select the host-accessible Control Block Registers.
Drive Active/Slave Present	DASP–	I/O	39	A time-multiplexed signal that indicates either drive activity or that drive 1 is present. During power-on initialization, DASP– is asserted by drive 1 within 400 ms to indicate that drive 1 is present. If drive 1 is not present, drive 0 asserts DASP– within 350 ms to light the drive-activity LED. An open-collector output signal, DASP– is deasserted following the receipt of a valid command by drive 1 or after the drive is ready, whichever occurs first. Once DASP– is deasserted, either hard drive can assert DASP– to light the drive-activity LED. Each drive has a 10K pull-up resistor on this signal. If an external drive-activity LED is used to monitor this signal, an external resistor must be connected in series between the signal and a +5 volt supply in order to limit the current to 24 mA maximum.
Ground	Ground	—	40	Ground between the host system and the drive.

6.4.1.3 IDE Bus Signals

See Table 6-2 for the relationship between the drive signals and the IDE bus.

Table 6-2 *Relationship of Drive Signals to the IDE Bus*

DRIVE CONNECTOR (J1)		DIRECTION	IDE BUS	
1	RESET–	<—(INV)	B2	RESET DRV
2	GROUND	—	—	GROUND
3	DD7	<—>	A2	SD7
4	DD8	<—>	C11	SD8
5	DD6	<—>	A3	SD6
6	DD9	<—>	C12	D9
7	DD5	<—>	A4	SD5
8	DD10	<—>	C13	SD10
9	DD4	<—>	A5	SD4
10	DD11	<—>	C14	SD11
11	DD3	<—>	A6	SD3
12	DD12	<—>	C15	SD12
13	DD2	<—>	A7	SD2
14	DD13	<—>	C16	SD13
15	DD1	<—>	A8	SD1
16	DD14	<—>	C17	SD14
17	DD0	<—>	A9	SD0
18	DD15	<—>	C18	SD15
19	GROUND	—	—	GROUND
20	KEYPIN	—	—	NO CONNECTION
21	DMARQ	—>	—[1]	DRQ
22	GROUND	—	—	GROUND
23	DIOW–	<—	B13	DIOW–
24	GROUND	—	—	GROUND
25	DIOR–	<—	B14	IOR–
26	GROUND	—	—	GROUND
27	IORDY	—>	A10	I/O CH RDY
28	CABLE SELECT	<—	—[2]	NO CONNECTION
29	DMACK–	<—	—[3]	DACK–
30	GROUND	—	—	GROUND
31	INTRQ	—>	D7	INTRQ
32	IOCS16–	—>	D2	I/O CS16–
33	ADDR1	<—	A30	SA1
34	PDIAG–	—	—	NO CONNECTION
35	DA0	<—	A31	SA0
36	ADDR2	<—	A29	SA2
37	CS1FX–	<—	—[4]	CS0–
38	CS3FX–	<—	—[4]	CS1–
39	DASP–	—	—[4]	NO CONNECTION
40	GROUND	—	—	GROUND

1. DMARQ from the drive must be jumpered to one of the DRQ lines on the motherboard or host adapter (normally connected to DRQ6).
2. Pin 28 is a vendor-specific pin that Quantum is using for a specific purpose. See Chapter 3 for details.
3. DACK– from the drive must be jumpered to one of the DACK– lines on the motherboard or host adapter (normally connected to DACK6–).
4. CS1FX–, CS3FX–, and DASP– originate on the adapter board.

6.4.2 Host Interface Timing

6.4.2.1 Programmed I/O (PIO) Transfer Mode

The PIO host interface timing shown in Table 6-3 is in reference to signals at 0.8 volts and 2.0 volts. All times are in nanoseconds, unless otherwise noted. Figure 6-1 provides a timing diagram.

Table 6-3 *PIO Host Interface Timing*

SYMBOL	DESCRIPTION	MIN/MAX	MODE 3[1] (local bus)	LIGHTNING AT
t0	Cycle Time	min	180	130
t1	Address Valid to DIOW–/DIOR–Setup	min	30	15
t2	DIOW–/DIOR– Pulsewidth (8- or 16-bit)	min	80	80
t2i	DIOW–/DIOR– Negated Pulsewidth	min	70	50
t3	DIOW–Data Setup	min	30	30
t4	DIOW– Data Hold	min	10	10
t5	DIOR– Data Setup	min	20	20
t5a	DIOR– to Data Valid	max	—	60
t6	DIOR– Data Hold	min	5	5
t6z	DIOR– Data Tristate	max	30	30
t7	Address Valid to IOCS16– Assertion	max	30	30
t8	Address Valid to IOSC16– Deassertion	max	30	30
t9	DIOW–/DIOR– to Address Valid Hold	min	10	10
tA	IORDY[2] Setup Time	min	35	35
tB	IORDY Pulse Width	max	—	1250
tR	Read Data Valid to IORDY active (if IORDY is initially low after tA)	min	0	0

1. ATA Mode 3 timing is listed for reference only.
2. Transfer rates above 7 MB/s require the use of IORDY.

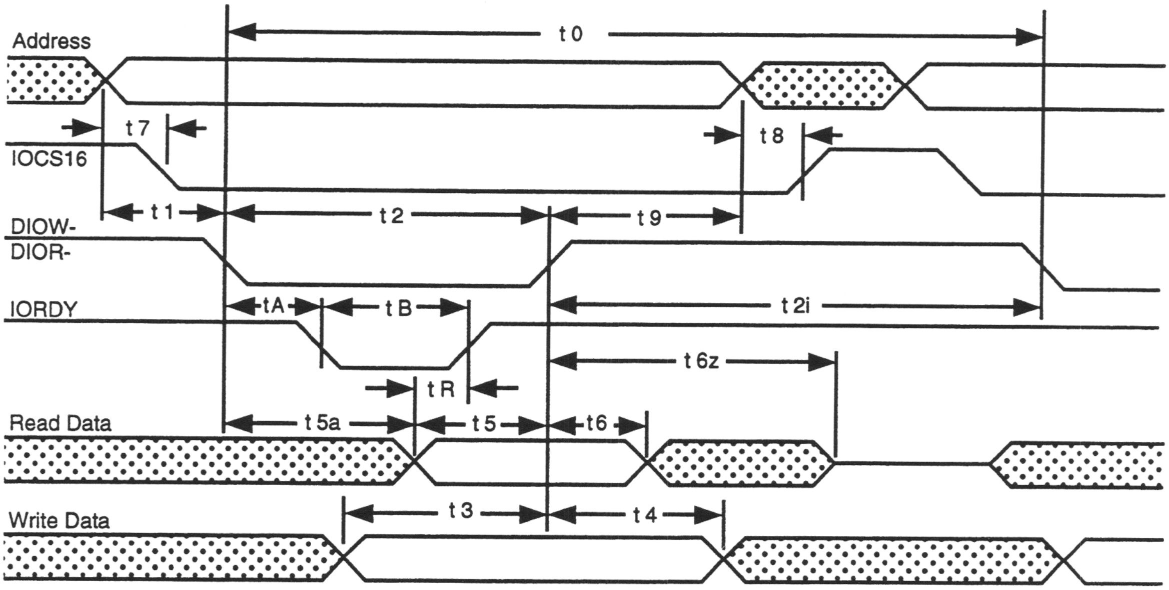

Figure 6-1 *PIO Interface Timing*

6.4.2.2 Multiword DMA Transfer Mode

The multiword DMA host interface timing shown in Table 6-4 is in reference to signals at 0.8 volts and 2.0 volts. All times are in nanoseconds, unless otherwise noted. Figure 6-2 provides a timing diagram.

Table 6-4 *Multiword DMA Host Interface Timing*

SYMBOL	DESCRIPTION	MIN/MAX	MODE 1[1] (local bus)	LIGHTNING AT
t0	Cycle Time	min	150	150
tD	DIOR–/DIOW– Pulsewidth	min	80	60
tE	DIOR– to Data Valid	max	60	60
tF	DIOR– Data Hold	min	5	5
tFz	DIOR– Data Tristate[2]	max	30	30
tG	DIOW– Data Setup	min	30	30
tH	DIOW– Data Hold	min	15	10
tI	DMACK to DIOR–/DIOW– Setup	min	0	0
tJ	DIOR–/DIOW– to DMACK– Hold	min	5	5
tK	DIOR–/DIOW– Negated Pulsewidth	min	50	50
tL	DIOR–/DIOW– to DMARQ Delay	max	40	40
tz	DMACK– Data Tristate[3]	max	25	25

1. ATA Mode 1 timing is listed for reference only.
2. The Lightning 365/540/730AT tristates after each word transferred.
3. Symbol tz only applies on the last tristate at the end of a multiword DMA transfer cycle.

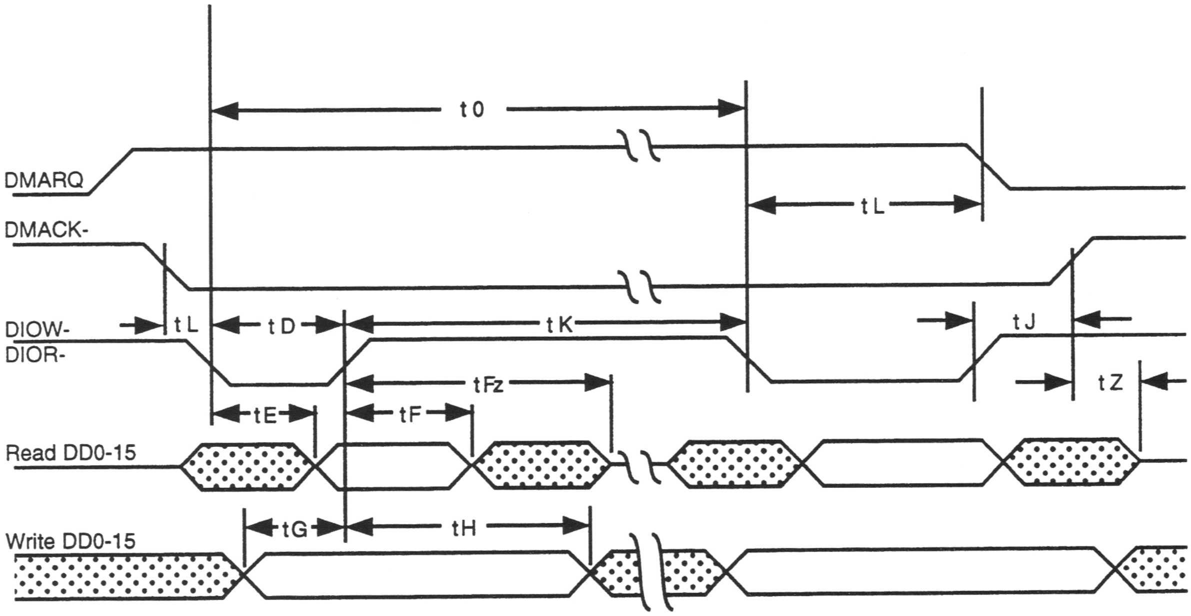

Figure 6-2 *Multiword DMA Bus Interface Timing*

6.4.2.3 Host Interface RESET Timing

The host interface RESET timing shown in Table 6-5 is in reference to signals at 0.8 volts and 2.0 volts. All times are in nanoseconds, unless otherwise noted. Figure 6-3 provides a timing diagram.

Table 6-5 *Host Interface RESET Timing*

SYMBOL	DESCRIPTION	MINIMUM	MAXIMUM
tM	RESET– Pulse width	300	—

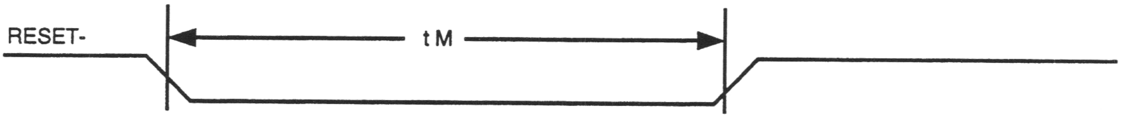

Figure 6-3 *Host Interface RESET Timing*

6.5 REGISTER ADDRESS DECODING

The host addresses the drive by using programmed I/O. Host address lines A0–A2, chip-select CS1FX– and CS3FX–, and IOR– and IOW– address the disk registers. Host address lines A3–A9 generate the two chip-select signals, CS1FX– and CS3FX–.

- Chip Select CS1FX– accesses the eight Command Block Registers.
- Chip Select CS3FX– is valid during 8-bit transfers to or from the Alternate Status Register.

The drive selects the primary or secondary command block addresses by setting Address bit A7.

Data bus lines 8–15 are valid only when IOCS16– is active and the drive is transferring data. The drive transfers ECC information only on data bus lines 0–7. Data bus lines 8–15 are invalid during transfers of ECC information.

I/O to or from the drive occurs over an I/O port that routes input or output data to or from selected registers, by using the following encoded signals from the host: CS1FX–, CS3FX–, DA2, DA1, DA0, DIOR–, and DIOW–. The host writes to the Command Block Registers when transmitting commands to the drive, and to the Control Block Registers when transmitting control, like a software reset. Table 6-6 lists the selection addresses for these registers.

Table 6-6 *I/O Port Functions and Selection Addresses*

FUNCTION		HOST SIGNALS				
CONTROL BLOCK REGISTERS		**CS1FX–**	**CS3FX–**	**DA2**	**DA1**	**DA0**
READ (DIOR–)	**WRITE (DIOW–)**					
Data Bus High Impedance	Not Used	N[1]	N	X[2]	X	X
Data Bus High Impedance	Not Used	N	A[3]	0	X	X
Data Bus High Impedance	Not Used	N	A	1	0	X
Alternate Status	Device Control	N	A	1	1	0
Drive Address	Not Used	N	A	1	1	1
COMMAND BLOCK REGISTERS						
READ (DIOR–)	**WRITE (DIOW–)**					
Data Port	Data Port	A	N	0	0	0
Error Register	Features	A	N	0	0	1
Sector Count	Sector Count	A	N	0	1	0
Sector Number[4]	Sector Number	A	N	0	1	1
LBA Bits 0–7[5]	LBA Bits 0–7	A	N	0	1	1
Cylinder Low[4]	Cylinder Low	A	N	1	0	0
LBA Bits 8–15[5]	LBA Bits 8–15	A	N	1	0	0
Cylinder High[4]	Cylinder High	A	N	1	0	1
LBA Bits 16–23[5]	LBA Bits 16–23	A	N	1	0	1
Drive/Head[4]	Drive/Head	A	N	1	1	0
LBA Bits 24–27[5]	LBA Bits 24–27	A	N	1	1	0
Status	Command	A	N	1	1	1
Invalid Address	Invalid Address	A	A	X	X	X

1. N = signal deasserted
2. X = signal either asserted or deasserted
3. A = signal asserted
4. Mapping of registers in CHS mode
5. Mapping of registers in LBA mode

After power on or following a reset, the drive initializes the Command Block Registers to the values shown in Table 6-7.

Table 6-7 *Command Block Register Initial Values*

REGISTER	VALUE
Error Register	01
Sector Count Register	01
Sector Number Register	01
Cylinder Low Register	00
Cylinder High Register	00
Drive/Head Register	00

6.6 REGISTER DESCRIPTIONS

The Lightning 365/540AT hard disk drive emulates the ATA Command and Control Block Registers. Functional descriptions of these registers are given in the next two sections.

6.6.1 Control Block Registers

6.6.1.1 Alternate Status Register

The Alternate Status Register contains the same information as the Status Register in the command block. Reading the Alternate Status Register does not imply the acknowledgment of an interrupt by the host or clear a pending interrupt. See the description of the Status Register in section 6.6.2.8 for definitions of bits in this register.

6.6.1.2 Device Control Register

This write-only register contains two control bits, as shown in Table 6-8.

Table 6-8 *Device Control Register Bits*

BIT	MNEMONIC	DESCRIPTION
7	Reserved	–
6	Reserved	–
5	Reserved	–
4	Reserved	–
3	1	Always 1
2	SRST[1]	Host software reset bit
1	nIEN[2]	Drive interrupt enable bit
0	0	Always 0

1. SRST = Host Software Reset bit. When the host sets this bit, the drive is reset. When two drives are daisy-chained on the interface, this bit resets both drives simultaneously.
2. nIEN = Drive Interrupt Enable bit. When nIEN equals 0 or the host has selected the drive, the drive enables the host interrupt signal INTRQ through a tristate buffer to the host. When nIEN equals 1 or the drive is not selected, the host interrupt signal INTRQ is in a high-impedance state, regardless of the presence or absence of a pending interrupt.

6.6.1.3 Drive Address Register

The Drive Address Register returns the head-select addresses for the drive currently selected. Table 6-9 shows the Drive Address bits.

Table 6-9 *Drive Address Register Bits*

BIT	MNEMONIC	DESCRIPTION
7	HiZ[1]	High Impedance bit
6	nWTG[2]	Write Gate bit
5	nHS3[3]	Head Address msb
4	nHS2	–
3	nHS1	–
2	nHS0	Head Address lsb
1	nDS1[4]	Drive 1 Select bit
0	nDS0	Drive 0 Select bit

1. HiZ = High Impedance bit. When the host reads the register, this bit will be in a high impedance state.
2. nWTG = Write Gate bit. When a write operation to the drive is in progress, nWTG equals 0.
3. nHS0–nHS3 = Head Address bits. These bits are equivalent to the one's complement of the binary-coded address of the head currently selected.
4. nDS0–nDS1 = Drive Select bits. When drive 1 is selected, nDS1 equals 0. When drive 0 is selected, nDS0 equals 0.

6.6.2 Command Block Registers

6.6.2.1 Data Port Register

All data transferred between the device data buffer and the host passes through the Data Port Register. The host transfers the sector table to this register during execution of the FORMAT TRACK command. Transfers of ECC bytes during the execution of READ LONG or WRITE LONG commands are 8-bit transfers.

6.6.2.2 Error Register

The Error Register contains status information about the last command executed by the drive. The contents of this register are valid only when the Error bit (ERR) in the Status Register is set to 1. The contents of the Error Register are also valid at power on, and at the completion of the drive's internal diagnostics, when the register contains a status code. When the error bit in the Status Register is set to 1, the host interprets the Error Register bits as shown in Table 6-10.

Table 6-10 *Error Register Bits*

MNEMONIC	BIT	DESCRIPTION
BBK	7	Bad block detected in the required sector's ID field.
UNC	6	Uncorrectable data error encountered.
–	5	Not used.
IDNF	4	Requested sector's ID field not found.
–	3	Not used.
ABRT	2	Requested command aborted due to a drive status error, such as Not Ready or Write Fault, or because the command code is invalid.
TKONF	1	Track 0 not found during execution of RECALIBRATE command.
AMNF	0	Data Address Mark not found after correct ID field format.

6.6.2.3 Sector Count Register

The Sector Count Register defines the number of sectors of data to be transferred across the host bus for a subsequent command. If the value in this register is 0, the sector count is 256 sectors. If the Sector Count Register command executes successfully, the value in this register at command completion is 0. As the drive transfers each sector, it decrements the Sector Count Register to reflect the number of sectors remaining to be transferred. If the command's execution is unsuccessful, this register contains the number of sectors that must be transferred to complete the original request.

When the drive executes an INITIALIZE DRIVE PARAMETERS or Format Track command, the value in this register defines the number of sectors per track.

6.6.2.4 Sector Number Register

The Sector Number Register contains the ID number of the first sector to be accessed by a subsequent command. The sector number is a value between one and the maximum number of sectors per track. As the drive transfers each sector, it increments the Sector Number Register. See the command descriptions in section 6.7 for information about the contents of the Sector Number Register after successful or unsuccessful command completion.

In LBA mode, this register contains bits 0 to 7. At command completion, the host updates this register to reflect the current LBA bits 0 to 7.

6.6.2.5 Cylinder Low Register

The Cylinder Low Register contains the eight low-order bits of the starting cylinder address for any disk access. On multiple sector transfers that cross cylinder boundaries, the host updates this register when command execution is complete, to reflect the current cylinder number. The host loads the least significant bits of the cylinder address into the Cylinder Low Register.

In LBA mode, this register contains bits 8 to 15. At command completion, the host updates this register to reflect the current LBA bits 8 to 15.

6.6.2.6 Cylinder High Register

The Cylinder High Register contains the eight high-order bits of the starting cylinder address for any disk access. On multiple sector transfers that cross cylinder boundaries, the host updates this register at the completion of command execution, to reflect the current cylinder number. The host loads the most significant bits of the cylinder address into the Cylinder High Register.

In LBA mode, this register contains bits 16 to 23. At command completion, the host updates this register to reflect the current LBA bits 16 to 23.

6.6.2.7 Drive/Head Register

The Drive/Head Register contains the drive ID number and its head numbers. By executing the INITIALIZE DRIVE PARAMETERS command, the host defines the contents of the Drive/Head Register.

In LBA mode, this register contains bits 24 to 27. At command completion, the host updates this register to reflect the current LBA bits 24 to 27.

Table 6-11 shows the Drive/Head Register bits.

Table 6-11 *Drive/Head Register Bits*

MNEMONIC	BIT	DESCRIPTION
Reserved	7[1]	Always *1*
L	6[2]	*0* for CHS mode *1* for LBA mode
Reserved	5	Always *1*
DRV	4[3]	*0* indicates the Master drive is selected *1* indicates the Slave drive is selected
HS3	3[4]	Most significant Head Address bit in CHS mode Bit 24 of the LBA Address in LBA mode
HS2	2	Head Address bit for CHS mode Bit 25 of the LBA Address in LBA mode
HS1	1	Head Address bit for CHS mode Bit 26 of the LBA Address in LBA mode
HS0	0	Least significant Head Address bit in CHS mode Bit 27 of the LBA Address in LBA mode

1. Bits 5–7 define the sector size set in hardware (512 bytes).
2. Bit 6 is the binary encoded Address Mode Select. When bit 6 is set to 0, addressing is by CHS mode. When bit 6 is set to 1, addressing is by LBA mode.
3. Bit 4 (DRV) contains the binary encoded drive select number. The Master is the primary drive; the Slave is the secondary drive
4. In CHS mode, bits 3–0 (HS0–HS3) contain the binary encoded address of the selected head. At command completion, the host updates these bits to reflect the address of the head currently selected. In LBA mode, bits 3–0 (HS0–HS3) contain bits 24–27 of the LBA Address. At command completion, the host updates this register to reflect the current LBA bits 24 to 27.

6.6.2.8 Status Register

The Status Register contains information about the status of the drive and the controller. The drive updates the contents of this register at the completion of each command. When the Busy bit is set (BSY=1), no other bits in the Command Block Registers are valid. When the Busy bit is not set (BSY=0), the information in the Status Register and Command Block Registers is valid.

When an interrupt is pending, the drive considers that the host has acknowledged the interrupt when it reads the Status Register. Therefore, whenever the host reads this register, the drive clears any pending interrupt. Table 6-12 defines the Status Register bits.

6.6.2.9 Command Register

The host sends a command to the drive by means of an 8-bit code written to the Command Register. As soon as the drive receives the command in its Command Register, it begins execution of the command. Table 6-13 lists the hexadecimal command codes and parameters for each executable command. The code F0h is common to all of the extended commands. Each of these commands is distinguished by a unique subcode. For a detailed description of each command, see Section 6.7, "COMMAND DESCRIPTIONS," found later in this chapter.

Table 6-12 *Status Register Bits*

MNEMONIC	BIT	DESCRIPTION
BSY	7	**Busy bit**. Set by the controller logic of the drive whenever the drive has access to and the host is locked out of the Command Block Registers. BSY is set under the following conditions: • Within 400 ns after the deassertion of RESET- or after SRST is set in the Device Control Register. Following a reset, BSY will be set for no longer than 30 seconds. • Within 400 ns of a host write to the Command Block Registers with a Read, READ LONG, READ BUFFER, SEEK, RECALIBRATE, INITIALIZE DRIVE PARAMETERS, Read Verify, Identify Drive, or EXECUTE DRIVE DIAGNOSTIC command. • Within 5 µsec after the transfer of 512 bytes of data during the execution of a Write, Format Track, or WRITE BUFFER command, or 512 bytes of data and the appropriate number of ECC bytes during the execution of a WRITE LONG command. When BSY=1, the host cannot write to a Command Block Register and reading any Command Block Register returns the contents of the Status Register.
DRDY	6	**Drive Ready bit**. Indicates that the drive is ready to accept a command. When an error occurs, this bit remains unchanged until the host reads the Status Register, then again indicates that the drive is ready. At power on, this bit should be cleared, and should remain cleared until the drive is up to speed and ready to accept a command.
DWF	5	**Drive Write Fault bit.** When an error occurs, this bit remains unchanged until the host reads the Status Register, then again indicates the current write fault status.
DSC	4	**Drive Seek Complete bit.** This bit is set when a seek operation is complete and the heads have settled over a track. When an error occurs, this bit remains unchanged until the host reads the Status Register, when it indicates the current seek-complete status.
DRQ	3	**Data Request bit.** When set, this bit indicates that the drive is ready to transfer a word or byte of data from the host to the data port.
CORR	2	**Corrected Data bit.** The drive sets this bit when it encounters and corrects a correctable data error. This condition does not terminate a multi-sector read operation.
IDX	1	**Index bit.** This bit is set when the drive detects the index mark, once per disk revolution.
ERR	0	**Error bit.** When set, this bit indicates that the previous command resulted in an error. The other bits in the Status Register and the bits in the Error Register contain additional information about the cause of the error.

Table 6-13 *Lightning 365/540/730AT Command Codes and Parameters*

COMMAND		PARAMETER				
NAME	**CODE**	**SC**	**SN**	**CY**	**DS**	**HD**
RECALIBRATE	1Xh				V	
READ SECTORS, with retry	20h	V	V	V	V	V
READ SECTORS, no retry	21h	V	V	V	V	V
READ LONG, with retry	22h	V	V	V	V	V
READ LONG, no retry	23h	V	V	V	V	V
WRITE SECTORS, with retry	30h	V	V	V	V	V
WRITE SECTORS, no retry	31h	V	V	V	V	V
WRITE LONG, with retry	32h	V	V	V	V	V
WRITE LONG, no retry	33h	V	V	V	V	V
READ VERIFY SECTORS, with retry	40h	V	V	V	V	V
READ VERIFY SECTORS, no retry	41h	V	V	V	V	V
FORMAT TRACK	50h	V		V	V	V
SEEK	7Xh		V	V	V	V
EXECUTE DRIVE DIAGNOSTIC	90h					
INITIALIZE DRIVE PARAMETERS	91h	V			V	V
READ MULTIPLE	C4h	V	V	V	V	V
WRITE MULTIPLE	C5h	V	V	V	V	V
SET MULTIPLE MODE	C6h	V			V	
READ DMA, with retry	C8h	V	V	V	V	V
READ DMA, no retry	C9h	V	V	V	V	V
WRITE DMA, with retry	CAh	V	V	V	V	V
WRITE DMA, no retry	CBh	V	V	V	V	V
STANDBY IMMEDIATE	E0h					V
IDLE IMMEDIATE	E1h					V
STANDBY MODE (AUTO POWER-DOWN)	E2h	V				V
IDLE MODE (AUTO POWER-DOWN)	E3h	V				V
READ BUFFER	E4h				V	
CHECK POWER MODE	E5h	V				V
SLEEP MODE	E6h					V
WRITE BUFFER	E8h				V	
IDENTIFY DRIVE	ECh				V	
READ DEFECT LIST—extended cmnd.	F0h	V	V	V	V	V
READ CONFIGURATION—extended cmnd.	F0h	V	V	V	V	V
SET CONFIGURATION—extended cmnd.	F0h	V	V	V	V	V

Note: The following information applies to Table 6-13:

SC = Sector Count Register
SN = Sector Number Register
CY = Cylinder Low and High Registers
DS = Drive Select bit (Bit 4 of Drive/Head Register)
HD = 3 Head Select Bits (Bits 0–3 of Drive Head Register)

V = Must contain valid information for this command

6.7 COMMAND DESCRIPTIONS

The Lightning 365/540/730AT hard disk drive supports all standard ATA drive commands. The drive decodes, then executes, commands loaded into the Command Block Register. In applications involving two hard drives, both drives receive all commands. However, only the selected drive executes commands—with the exception of the EXECUTE DRIVE DIAGNOSTIC command, as explained below. The procedure for executing a command on the selected drive is as follows:

1. Wait for the drive to indicate that it is no longer busy (BSY=0).
2. Load the required parameters into the Command Block Register.
3. Activate the Interrupt Enable (–IEN) bit.
4. Wait for the drive to set RDY (RDY=1).
5. Write the command code to the Command Register.

Execution of the command begins as soon as the drive loads the Command Block Register. The remainder of this section describes the function of each command. The commands are listed in the same order they appear in Table 6-13.

6.7.1 Recalibrate

The RECALIBRATE command moves the read/write heads from any location on the disk to cylinder 0. On receiving this command, the drive sets the BSY bit and issues a seek command to cylinder 0. The drive then waits for the seek operation to complete, updates status, negates BSY, and generates an interrupt. If the drive cannot seek to cylinder 0, it posts the message TRACK 0 NOT FOUND.

6.7.2 Read Sectors

The Read Sectors command reads from 1 to 256 sectors, beginning at the specified sector. As specified in the Command Block Register, a sector count equal to 0 requests 256 sectors. When the drive accepts this command, it sets BSY and begins execution of the command.

6.7.2.1 Read Long

When the Long bit is set in the command code, a READ LONG command executes, returning the data and the ECC bytes contained in the data field of the requested sector. During a READ LONG operation, the drive does not check the ECC bytes to determine if a data error of any kind has occurred.

6.7.2.2 Multiple Sector Reads

Multiple sector reads set DRQ. After reading each sector, the drive generates an interrupt when the sector buffer is full and the drive is ready for the host to read the data. Once the host empties the sector buffer, the drive immediately clears DRQ and sets BSY.

If an error occurs during a multiple sector read, the read terminates at the sector in which the error occurred. The Command Block Register contains the cylinder, head, and sector numbers of the sector in which the error occurred. The host can then read the Command Block Register to determine what kind of error has occurred, and in which sector. Whether the data error is correctable or uncorrectable, the drive loads the data into the sector buffer.

6.7.3 Write Sector

The WRITE SECTOR command writes from 1 to 256 sectors, beginning at the specified sector. As specified in the Command Block Register, a sector count equal to 0 requests 256 sectors. When the drive accepts this command, it sets DRQ and waits for the host to fill the sector buffer with the data to be written to the drive. The drive does not generate an interrupt to start the first buffer-fill operation. Once the buffer is full, the drive clears DRQ, sets BSY, and begins execution of the command.

6.7.3.1 Write Long

When the Long bit is set in the command code, a WRITE LONG command writes the data and the ECC bytes directly from the sector buffer. The drive does not generate the ECC bytes itself.

6.7.3.2 Multiple Sector Writes

The MULTIPLE SECTOR WRITES command sets DRQ. The drive generates an interrupt whenever the sector buffer is ready to be filled. When the host fills the sector buffer, the drive immediately clears DRQ and sets BSY.

If an error occurs during a multiple sector write operation, the write operation terminates at the sector in which the error occurred. The Command Block Register contains the cylinder, head, and sector numbers of the sector in which the error occurred. The host can then read the Command Block Register to determine what kind of error has occurred, and in which sector.

6.7.4 Read Verify Sectors

The execution of the READ VERIFY SECTORS command is identical to that of the READ SECTORS command. However, the Read Verify command does not cause the drive to set DRQ, the drive transfers no data to the host, and the Long bit is invalid. On receiving the READ VERIFY command, the drive sets BSY. When the drive has verified the requested sectors, it clears BSY and generates an interrupt. On command completion, the Command Block Registers contain the cylinder, head, and sector numbers of the last sector verified.

If an error occurs during a multiple sector verify operation, the read operation terminates at the sector in which the error occurred. The Command Block Registers contain the cylinder, head, and sector numbers in which the error occurred.

6.7.5 Format Track

The host specifies the track addresses by writing to the Cylinder and Head Registers. When the drive accepts a FORMAT TRACK command, it sets the DRQ bit, then waits for the host to fill the sector buffer. When the buffer is full, the drive clears DRQ, sets BSY, and begins command execution. The contents of the sector buffer are not written to the disk, and may be ignored or interpreted as shown in Table 6-14.

Table 6-14 *Sector Buffer Contents*

DD15 --- DD0		**DD15 --- DD0**	
First Sector Descriptor	: : : : : : : : : : : : : :	Last Sector Descriptor	Remainder of buffer filled with zeros

On the Lightning 365/540/730AT hard disk drive, the FORMAT TRACK command writes zeros to the data fields in the sectors on the specified logical track. The drive writes no headers at these locations. The Sector Count register contains the number of sectors per track.

One 16-bit word represents each sector (the words are contiguous from the start of the sector).

Note: Any words remaining in the buffer after the representation of the last sector must be filled with zeros.

DD15–8 contain the sector number. DD7–0 contain a descriptor value that is defined below. The words must appear in sequential order starting at sector one and ending on the last sector number of the track.

• 00h	Format sector as good
• 20h	Unassign the alternate location for this sector
• 40h	Assign this sector to an alternate location
• 80h	Format sector as bad

6.7.6 Seek

The SEEK command causes the actuator to seek to the track to which the Cylinder and Drive/Head registers point. When the drive receives this command in its Command Block Registers, it performs the following functions:

1. Sets BSY
2. Initiates the seek operation
3. Resets BSY
4. Sets the Drive Seek Complete (DSC) bit in the Status Register

The drive does not wait for the seek to complete before it sends an interrupt. If the BSY bit is *not* set in the Status Register, the drive can accept and queue subsequent commands while performing the seek. If the Cylinder registers contain an illegal cylinder, the drive sets the ERR bit in the Status Register and the IDNF bit in the Error Register.

6.7.7 Execute Drive Diagnostic

The EXECUTE DRIVE DIAGNOSTIC command performs the internal diagnostic tests implemented on the drive. Drive 0 sets BSY within 400 ns of receiving of the command.

If Drive 1 is present:

- Both drives execute diagnostics.
- Drive 0 waits up to six seconds for drive 1 to assert PDIAG–.
- If drive 1 does not assert PDIAG– to indicate a failure, drive 0 appends 80h with its own diagnostic status.
- If the host detects a drive 1 diagnostic failure when reading drive 0 status, it sets the DRV bit, then reads the drive 1 status.

If Drive 1 is not present:

- Drive 0 reports only its own diagnostic results.
- Drive 0 clears BSY and generates an interrupt.

If drive 1 fails diagnostics, drive 0 appends 80h with its own diagnostic status and loads that code into the Error Register. If drive 1 passes its diagnostics or no drive 1 is present, drive 0 appends 00h with its own diagnostic status and loads that code into the Error Register.

The diagnostic code written to the Error Register is a unique 8-bit code. Table 6-15 lists the diagnostic codes.

Table 6-15 *Diagnostic Codes*

DIAGNOSTIC CODE	DESCRIPTION
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Drive 1 Failed

6.7.8 Initialize Drive Parameters

The INITIALIZE DRIVE PARAMETERS command enables the host to set the logical number of heads and the logical number of sectors per track. On receiving the command, the drive sets the BSY bit, saves the parameters, clears BSY, and generates an interrupt.

The only two register values used by this command are the Sector Count Register, which specifies the number of sectors; and the Drive/Head Register, which specifies the number of heads, minus 1. The DRV bit assigns these values to drive 0 or drive 1, as appropriate.

This command does not check the sector count and head values for validity. If these values are invalid, the drive will not report an error until another command causes an illegal access.

6.7.9 Read Multiple

The execution of the READ MULTIPLE command is identical to that of the Read Sectors command. However, the READ MULTIPLE command:

- Transfers blocks of data to the host without intervening interrupts
- Requires DRQ qualification of the transfer only at the start of the block—*not* at each sector
- Invalidates the Long bit

The SET MULTIPLE MODE command specifies the block count, or the number of sectors to be transferred as a block. This command executes prior to the READ MULTIPLE command. When the host issues a READ MULTIPLE command, the Sector Count Register contains the number of sectors requested—not the number of blocks or the block count.

If this sector count is not evenly divisible by the block count, the drive transfers as many full blocks as possible to the host, followed by a final partial-block transfer. The partial-block transfer is for *n* sectors, where:

n = (sector count) modulo (block count)

If the drive attempts execution of a READ MULTIPLE command before executing the SET MULTIPLE MODE command or if READ MULTIPLE commands are disabled, an abort command error occurs.

The drive reports disk errors encountered during READ MULTIPLE commands at the beginning of a block or partial-block transfer. However, the drive still sets DRQ and transfers the data—including any corrupted data.

6.7.10 Write Multiple

The execution of the WRITE MULTIPLE command is identical to that of the Write Sectors command. However, the WRITE MULTIPLE command:

- Causes the controller to set BSY within 400 nsec of accepting the command
- Causes the drive to transfer multiple-sector blocks of data to the drive without intervening interrupts
- Requires DRQ qualification of the transfer only at the start of the block, not at each sector
- Invalidates the Long bit

The SET MULTIPLE MODE command specifies the block count, or the number of sectors to be transferred as a block. This command executes prior to the WRITE MULTIPLE command. When the host issues a WRITE MULTIPLE command, the Sector Count Register contains the number of sectors requested—not the number of blocks or the block count.

If this sector count is not evenly divisible by the block count, the drive transfers as many full blocks as possible, followed by a final partial-block transfer. The partial-block transfer is for n sectors, where:

$$n = (\text{sector count}) \text{ modulo } (\text{block count})$$

If the drive attempts to execute a WRITE MULTIPLE command before executing the SET MULTIPLE MODE command or while WRITE MULTIPLE commands are disabled, an Abort Command error occurs.

During the execution of a WRITE MULTIPLE command, the drive reports all disk errors encountered, following an attempted disk write of the block or partial block. When an error occurs, the WRITE MULTIPLE command ends at the sector that contains the error—even if it is in the middle of a block—and does not transfer subsequent blocks. The drive generates interrupts by setting DRQ at the beginning of each block or partial block.

6.7.11 Set Multiple Mode

The SET MULTIPLE MODE command enables the controller to perform READ MULTIPLE and WRITE MULTIPLE operations, and establishes the block count for these commands.

Prior to issuing a command, the host should load the Sector Count Register with the number of sectors per block. On receiving this command, the drive sets BSY and checks the contents of the Sector Count Register.

If the Sector Count Register contains a valid value and the controller supports block count, the controller loads the values for all subsequent READ MULTIPLE and WRITE MULTIPLE commands and enables execution of these commands. Any unsupported block count in the register causes an Aborted Command error, and disables execution of READ MULTIPLE and WRITE MULTIPLE commands.

If the Sector Count Register contains a zero value when the host issues the command, READ MULTIPLE and WRITE MULTIPLE commands are disabled. Any unsupported block count in the register causes an aborted command error, and disables READ MULTIPLE and WRITE MULTIPLE commands. After the command is executed, the controller clears BSY. At power on, or after a software or hardware reset, the default mode for the READ MULTIPLE and WRITE MULTIPLE commands is disabled.

6.7.12 Read Buffer

The READ BUFFER command enables the host to read the current contents of the drive's sector buffer. When the host issues this command, the drive sets BSY, sets up the sector buffer for a read operation, sets DRQ, clears BSY, and generates an interrupt. The host then reads up to 512 bytes of data from the buffer.

The drive can synchronize READ BUFFER and WRITE BUFFER commands from the host; that is, sequential READ BUFFER and WRITE BUFFER commands can access the same 512 bytes within the buffer.

6.7.13 Write Buffer

The WRITE BUFFER command allows the host to write the first 512 bytes of the drive's buffer. On receiving this command in its Command Block Register, the drive sets BSY and prepares for a write operation. When ready, the drive sets DRQ, resets BSY, and generates INTRQ, allowing the host to write to the buffer.

6.7.14 Power Management Commands

The Lightning 365/540/730AT provides numerous power management options. Two important options center around a count down counter known as the automatic power down counter or APD. This counter can trigger one of two power saving events depending upon which of the two commands was most recently issued:

- **Standby:**
  Once a standby command is issued, the drive enters the standby mode. Further, each time the APD counter reaches zero in the future, the drive enters the standby mode. In the standby mode, the spindle and actuator motors are off and the heads are parked in the landing zone. Receipt of any command that requires media access causes the drive to exit the standby command and service the host request. Each time the drive executes the standby command, the drive will reenter the standby mode when the APD counter reaches zero.
- **Idle:**
  Once an idle command is issued, each time the APD counter reaches zero, the drive enters the Standby mode. In the standby mode, the actuator and spindle motors are off with the heads locked in the landing area. This is the default setting.
- **Automatic Power Down (APD) Mode:**
  When in APD mode, the drive transitions to Standby Mode when the APD time elapses. Receipt of any command that requires media access causes the drive to exit Standby Mode. Upon receiving a command, the drive resets the APD counter to zero and starts it over again (with the exception of the Check Power Mode command, which does not reset the APD counter).

Three commands are available which are not dependent upon the APD counter reaching zero:

- **Sleep:** When a sleep command is received, the drive enters the sleep mode. In the sleep mode, the spindle and actuator motors are off and the heads are latched in the landing zone. Receipt of a reset causes the drive to transition from the sleep to the standby mode.
- **Standby Immediate:** When a standby immediate command is received, the drive immediately enters the standby mode.
- **Idle Immediate:** When an idle immediate command is received, after the first decrement of the APD counter, the drive enters the idle mode.

The sleep, standby immediate, and idle immediate commands differ in a significant way from the standby and idle commands. Specifically, sleep, standby immediate, and idle immediate have a one-time effect and must be reissued each time their effect is desired. In contrast, standby and idle operate in conjunction with the APD counter and stay in effect continually, becoming non-effectual only upon issuance of the other of these two commands. Thus, for example, once the standby command is issued just one time, each time the APD counter reaches zero the drive will enter the standby mode.

SECTOR COUNT	TIME
0	APD disable
1 - 240	(Value X 5) seconds
241 - 251	((Value – 240) X 30 minutes)
252	21 minutes
253	8 - 12 hours (Vendor unique)
254	Reserved
255	21 minutes and 15 seconds

6.7.14.1 Standby Immediate Mode – E0h

The Standby Immediate Mode power command immediately puts the drive in the Standby Mode. Power is removed from the spindle motor (the drive's PCB power remains) and the heads are parked.

6.7.14.2 Idle Immediate Mode – E1h

The Idle Immediate Mode power command immediately puts the drive in the Idle Mode.

6.7.14.3 Standby Mode, Automatic Power-Down – E2h

The Standby Mode, Automatic Power-Down (APD) command immediately puts the drive in the Standby Mode. The Sector Count Register is then examined. If the value in this register is not zero, the Auto Power-Down feature is enabled and will take effect once the countdown timer reaches zero. Each count represents a five second increment. The valid count range is from 12 to 255. Each time the drive is accessed, the countdown timer is reset to the value originally set in the Sector Count Register at the time the Standby Mode-Auto Power Down command was issued.

Note: If the value in the Sector Count Register is zero, the Auto Power-Down feature is disabled.

6.7.14.4 Idle Mode, Automatic Power-Down – E3h

The Idle Mode, Automatic Power-Down command immediately puts the drive into the Idle Mode. The Sector Count Register is then examined. If the value in this register is not zero, the Auto Power-Down feature is enabled and takes effect once the countdown timer reaches zero. Each count represents a five second increment. The valid count range is from 12 to 255. Each time the drive is accessed, the countdown timer is reset to the value originally set in the Sector Count Register at the time the Idle Mode-Auto Power Down command was issued.

Note: If the value in the Sector Count Register is zero, the Auto Power-Down feature is disabled.

6.7.14.5 Check Power Mode – E5h

The CHECK POWER MODE command writes FFh into the Sector Count Register provided that the drive is in the Idle Mode, even if it is in Automatic Power-Down mode. However, if it is in Standby mode, the drive returns a value of 00h in the Sector Count Register.

6.7.14.6 Sleep Mode – E6h

The Lightning drive considers the Sleep Mode to be the equivalent to the Standby Mode, except that a reset is required before issuing a command requiring media access.

6.7.15 Identify Drive

The IDENTIFY DRIVE command enables the host to receive parameter information from the drive. When the host issues this command, the drive sets BSY, stores the required parameter information in the sector buffer, sets DRQ, and generates an interrupt. The host then reads the information from the sector buffer. The Identify Drive Parameters Table, shown in Table 6-16, defines the parameter words stored in the buffer. All reserved bits should be zeros. A full explanation of the parameter words is listed below:

Default Logical Cylinders: The number of translated cylinders in the default translation mode.

Number of Logical Heads: The number of translated heads in the default translation mode.

Number of Unformatted Bytes Per Track: The number of unformatted bytes per translated track in the default translation mode.

Number of Unformatted Bytes Per Sector: The number of unformatted bytes per sector in the default translation mode.

Number of Logical Sectors Per Track: The number of sectors per track in the default translation mode.

Serial Number: The contents of this field are left aligned and padded with spaces (20h).

Buffer Type: The contents of this field are as follows:

- 0000h = Not specified
- 0001h = A single-ported, single-sector buffer capable of data transfers either to or from the host or to or from the disk
- 0002h = A dual-ported, multiple-sector buffer capable of simultaneous data transfers either to and from the host, or from the host and the disk
- 0003h = A dual-ported, multiple-sector buffer capable of simultaneous data transfers with read caching
- 0004 – FFFFh = Reserved

Firmware Revision: The contents of this field are left-aligned and padded with spaces (20h).

Model Number: The contents of this field are left-aligned and padded with spaces (20h). The low-order byte appears first in a word.

Table 6-16 *Identify Drive Parameters*

WORDS[1]			PARAMETER DESCRIPTION (Statements below are true if the bit is set to 1)
WORD	BIT	BIT VALUE	
0	15	0	Reserved for nonmagnetic drives
	14	0	Format speed tolerance gap required
	13	0	Track offset option available
	12	0	Data strobe offset option available
	11	1	Rotational speed tolerance is > 0.5%
	10	0	Disk transfer rate > 10 Mbit/s
	9	1	Disk transfer rate > 5 Mbit/s, but < 10 Mbit/s
	8	0	Disk transfer rate <= 5 Mbit/s
	7	0	Reserved for removable-cartridge drive
	6	1	Hard disk drive
	5	0	Spindle motor control option implemented
	4	1	Head-switch time > 15 µs
	3	1	Not MFM-encoded
	2	0	Soft-sectored
	1	1	Hard-sectored
	0	0	Reserved
1		365AT = 976 540AT = 1,120 730 AT = 1,416	Default logical cylinders
2		0	Reserved

WORDS[1]			PARAMETER DESCRIPTION (Statements below are true if the bit is set to 1)
WORD	**BIT**	**BIT VALUE**	
3		365AT = 12 540AT = 16 730 AT = 16	Number of logical heads
4		365AT = 31,232 540AT = 30,208 730 AT = 32,256	Number of unformatted bytes per track
5		512	Number of unformatted bytes per sector
6		365AT = 61 540AT = 59 730 AT = 63	Number of logical sectors per track
7–9		5154h	Vendor-unique
10–19			Serial number (20 ASCII characters)[2]
20		3	Buffer type
21		192	Buffer size in 512-byte increments
22		4	Number of ECC bytes passed on READ/WRITE LONG commands
23–26			Firmware revision (8 ASCII characters)
27–46			Model number (40 ASCII characters)
47	15–8 7–0	80h 08h	Vendor Unique Maximum number of sectors that can be transferred per interrupt is set to 8 for READ MULTIPLE and WRITE MULTIPLE commands.
48		0	Cannot perform double word I/O
49	15–12	0	Reserved
	11	1	1 = I/O Ready is supported
	10	1	1 = I/O Ready can be disabled
	9	1	1 = LBA supported
	8	1	1 = DMA supported
	7–0	0	Vendor Unique
50		0	Reserved
51	15–8	2	PIO data-transfer cycle timing mode
	7–0	0	Vendor Unique
52	15–8	2	DMA data-transfer cycle timing mode
	7–0	o	Vendor Unique
53	15–2	0	Reserved
	1	1	1 = The fields in words 64–70 are valid
	0	1	1 = The fields in words 54–58 are valid
54		365AT = 976 540AT = 1,120 730 AT = 1,416	Number of current cylinders
55		365AT = 12 540AT = 16 730 AT = 16	Number of current heads

WORDS[1]			PARAMETER DESCRIPTION (Statements below are true if the bit is set to 1)
WORD	**BIT**	**BIT VALUE**	
56		365AT = 61 540AT = 59 730 AT = 63	Number of current sectors per track
57–58		365AT = 714,432 540AT = 1,057,280 730 AT = 1,427,328	Current capacity in sectors
59	15–9 8 7–0	0 1 n[3]	Reserved Multiple sector setting is valid Current setting for number of sectors that can be transferred per interrupt on R/W Multiple commands
60–61		365AT = 714,432 540AT = 1,057,280 730 AT = 1,427,328	Total number of User Addressable Sectors (LBA Mode only)
62	15–8 7–0	4 7	Single-word DMA transfer mode active (Mode 2) Single-word DMA transfer modes supported (Mode 2)
63	15–8 7–0	2 3	Multiword DMA transfer mode active (Mode 1) Multiword DMA transfer modes supported (Mode 1)
64		1	Advanced PIO Mode is supported
65		150	Minimum multiword DMA transfer cycle time (ns) per word
66		150	Manufacturer's recommended multiword DMA cycle time (ns)
67		333	Manufacturer's PIO cycle time (ns) without flow control
68		180	Manufacturer's PIO cycle time (ns) with flow control

1. The format of an ASCII field specifies that, within a word boundary, the low-order byte appears first.
2. The serial number has the following format: 00QTMTCYJJJLSSSSBBB

where:
00 = Placeholders
QT = Quantum
M = Place of manufacture
T = Drive type family (fixed at 2)
C = Drive capacity (3 = 365 MB, 5 = 540 MB, 7 = 730 MB)
Y = Last digit of year drive built
JJJ = Julian day
L = Manufacturing production line
SSSS = Sequence of manufacture
BBB = Blanks (placeholders)

3. n is a variable from zero to eight.

6.7.16 Set Features

The SET FEATURES command is used by the host to establish certain parameters which control execution of the following drive features:

- 02h – Enable write cache feature
- 55h – Disable read look-ahead feature
- 82h – Disable write cache feature
- AAh – Enable read look-ahead feature

At power-on, or after a reset accomplished by either the hardware or software, the default mode is 4 bytes of ECC and read look-ahead.

6.7.17 Read Defect List

The READ DEFECT LIST command enables the host to retrieve the drive's defect list. When the host writes the bytes at addresses 1F2H–1F6H, followed by F0h at address 1F7h, the drive sets BSY, retrieves the defect list, sets DRQ, and resets BSY. The first byte, 04h, is a subcode to the extended command code F0h. The host can now read five sectors (512 bytes) of data. An INTRQ precedes each sector. Table 6-17 lists the bytes for this command.

Table 6-17 *READ DEFECT LIST Command Bytes*

ADDRESS	VALUE	DEFINITION
1F2	05h	Defect List Subcode
1F3	FFh	Password
1F4	FFh	Password
1F5	3Fh	Password
1F6	AXh (Drive 0)	Drive Select
	BXh (Drive 1)	—
1F7	F0h	Extended Command Code

In Table 6-17:

- Registers 1F2h through 1F5h must contain the exact values shown. These values function as a key. The drive issues the message ILLEGAL COMMAND if the bytes are not entered correctly.
- To select the proper drive, set register 1F6h. For execution of the command to begin, load register 1F7h with F0h.

The seven bytes listed in Figure 6-4 describe each defect or replacement in a physical cylinder, head, and sector.

6.7.18 Defect List Data Structure

The defect lists maintained and accessed by the defect management system consist of 6 byte defect entries. The P list contains only defect entries while the W list contains both defect and replacement cylinder information. The defect list structure is illustrated in Figure 6-4.

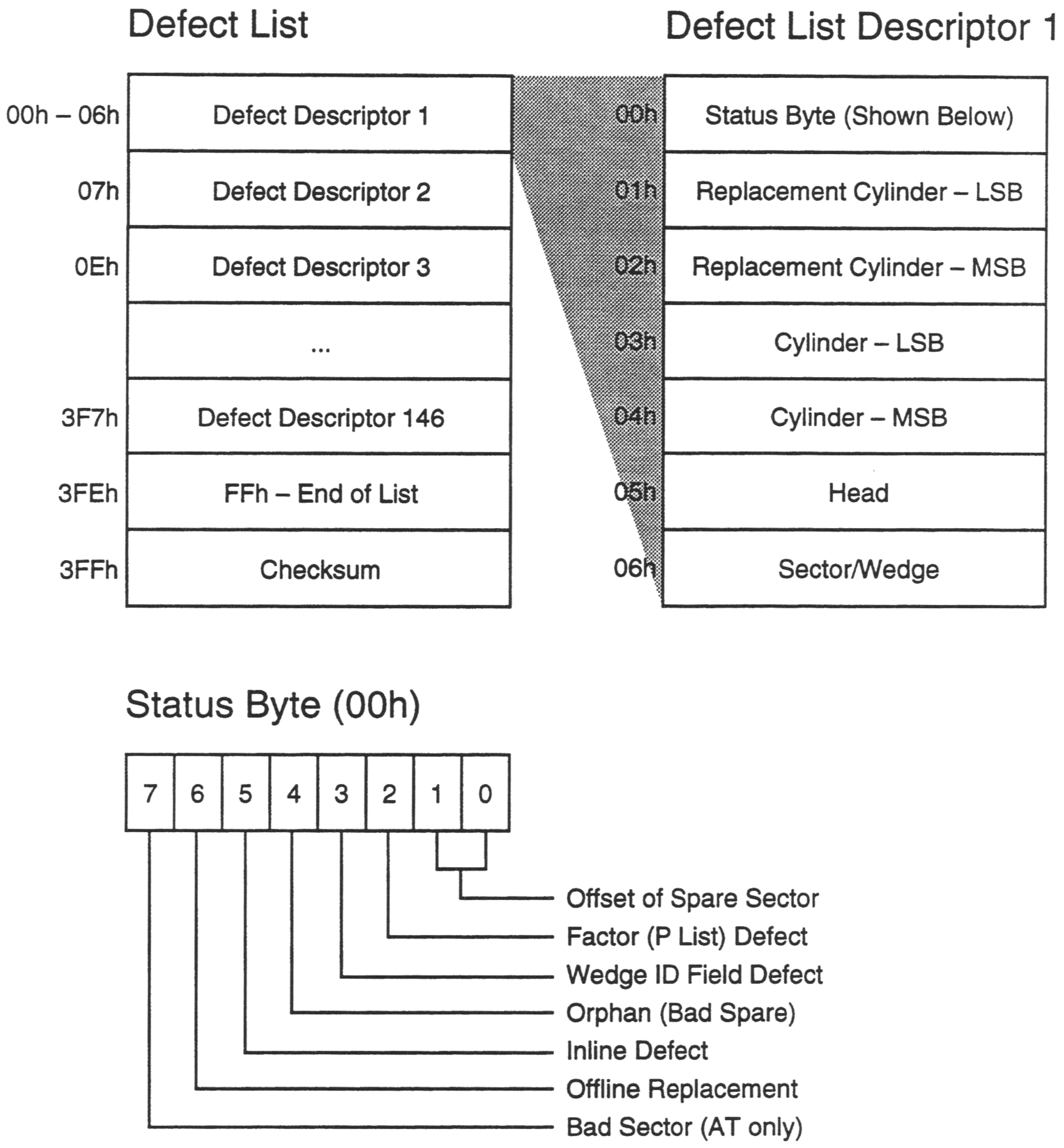

Figure 6-4 *Defect List Data Structure*

The end of list marker is placed after the last entry in the list (i.e., if there is only one defect, the end of list marker would be located at byte 07h).

The checksum is placed at the end of the list, and the empty area in the list is filled with zeros. When this byte is added to the rest of the bytes in the list, the **lsb** of the checksum will equal ASCII "L".

Table 6-18 shows a sample defect list.

Table 6-18 *Sample Defect List*

ENTRY	VALUE	DESCRIPTION
Defect Descriptor 1	A4h	Factory-found defect—spared inline transparently
	07h	Replacement Cylinder = 07 (LSB)
	00h	Replacement Cylinder = 00 (MSB)
	07h	Defective Cylinder = 07
	00h	Defective Cylinder = 00 (MSB)
	00h	Defective Head = 00
	02h	Defective Sector = 02
Defect	82h	Field-found defect—automatically reallocated offline
	08h	Replacement Cylinder = 08
	00h	Replacement Cylinder = 00 (MSB)
	07h	Defective Cylinder = 07
	00h	Defective Cylinder = 00 (MSB)
	01h	Defective head = 01
	04h	Defective sector = 04
	FFh	End of list marker

6.7.19 Configuration

In addition to the SET FEATURES command, the Lightning 365/540/730AT hard disk drive provides two configuration commands:

- The SET CONFIGURATION command, which enables the host to change DisCache and Error Recovery parameters
- The READ CONFIGURATION command, which enables the host to read the current configuration status of the drive

See Chapter 5 for more details about DisCache and setting cache parameters. See Chapter 5 also for more information about error detection and defect management.

6.7.19.1 Read Configuration

The READ CONFIGURATION command displays the configuration of the drive. Like the SET CONFIGURATION command, this command is secured to prevent accidentally accessing it. To access the READ CONFIGURATION command, you must write the pattern shown inTable 6-19 to the Command Block Registers. The first byte, 01h, is a subcode to the extended command code, F0h.

Table 6-19 *Accessing the READ CONFIGURATION Command*

ADDRESS	VALUE	DEFINITION
1F2h	01h	Read Configuration Subcode
1F3h	FFh	Password
1F4h	FFh	Password
1F5h	3Fh	Password
1F6h	AXh (Drive 0)	Drive Select
	BXh (Drive 1)	Drive Select
1F7h	F0h	Extended Command Code

Note: In Table 6-19:

Only the value in address 1F2h of the Command Block Registers is different from the SET CONFIGURATION command.

Registers 1F2h through 1F5h must contain the exact values shown in Table 6-19. These values function as a key. The drive issues the message ILLEGAL COMMAND if the key is not entered correctly.

To select the drive for which the configuration is to be read, set register 1F6h. For execution of the command to begin, load register 1F7h with F0h.

A 512-byte data field is associated with the READ CONFIGURATION command. A 512-byte read sequence sends this data from the drive to the host. The information in this data field represents the current settings of the configuration parameters. The format of the READ CONFIGURATION command data field is similar to that for the data field of the SET CONFIGURATION command, shown in Table 6-20. However, in the READ CONFIGURATION command, bytes 0 through 31 of the data field are *not* KEY information, as they are in the SET CONFIGURATION command. The drive reads these bytes as *QUANTUM CONFIGURATION,* followed by eleven spaces. Users can read the configuration into a buffer, then alter the configuration parameter settings.

6.7.19.2 Set Configuration

The SET CONFIGURATION command is secured to prevent accessing it accidentally. To access the SET CONFIGURATION command, you must write the pattern shown in Table 6-20 to the Command Block Registers. The first byte, FFh, is a subcode to the extended command code F0h.

Table 6-20 *Accessing the SET CONFIGURATION Command*

ADDRESS	VALUE	DEFINITION
1F2h	FFh	Set Configuration Subcode
1F3h	FFh	Password
1F4h	FFh	Password
1F5h	3Fh	Password
1F6h	AXh (Drive 0)	Drive Select
	BXh (Drive 1)	Drive Select
1F7h	F0h	Extended Command Code

Note: In Table 6-20:
Registers 1F2h through 1F5h must contain the exact values shown above. These values function as a key. The drive issues the message ILLEGAL COMMAND if the key is not entered correctly.
To select the drive being reconfigured, register 1F6h should be set. For execution of the command to begin, load register 1F7h with F0h.

6.7.19.3 Set Configuration Without Saving to Disk

The SET CONFIGURATION WITHOUT SAVING TO DISK command is secured to prevent accidentally accessing it. To access this command, you must write the pattern shown in Table 6-21 to the Command Block Registers. The first byte, FFh, is a subcode to the extended command code F0h.

Table 6-21 *Accessing the SET CONFIGURATION WITHOUT SAVING TO DISK Command*

ADDRESS	VALUE	DEFINITION
1F2h	FEh	Set Configuration Subcode
1F3h	FEh	Password
1F4h	FEh	Password
1F5h	3Fh	Password
1F6h	AXh (Drive 0)	Drive Select
	BXh Drive 1)	Drive Select
1F7h	F0h	Extended Command Code

Note: In Table 6-21:
Registers 1F2h through 1F5h must contain the exact values shown above. These values function as a key. The drive issues the message ILLEGAL COMMAND if the key is not entered correctly.
To select the drive being reconfigured, set register 1F6h. For execution of the command to begin, load register 1F7h with F0h.

6.7.19.4 Configuration Command Data Field

A 512-byte data field is associated with this command. This data field is sent to the drive through a normal 512-byte write handshake. Table 6-22 shows the format of the data field. Bytes 0 through 31 of the data field contain additional KEY information. The drive issues the message ILLEGAL COMMAND if this information is not entered correctly. Bytes 32 through 35 control the operation of DisCache. Bytes 36 through 38 control operation of the error recovery procedure. The drive does not use bytes 40 through 511, which should be set to 0.

Table 6-22 *Configuration Command Format*

BYTE	BIT							
	7	6	5	4	3	2	1	0
0–31	QUANTUM CONFIGURATION KEY							
32	RESERVED = 0						PE	CE
33	NUMBER OF CACHE SEGMENTS							
34	RESERVED = 0							
35	RESERVED = 0							
36	AWRE	ARR	N/A	RC	EEC	N/A	N/A	DCR
37	NUMBER OF RETRIES							
38	ECC CORRECTION SPAN							
39	RESERVED = 0	AR	ACHS	0	0	WCE	RUEE	0
40–511	RESERVED = 0							

Note: All fields marked RESERVED or N/A should be set to zero.

6.7.19.5 Quantum Configuration Key (Bytes 0-31)

Bytes 0–6 must contain the ASCII characters *Q, U, A, N, T, U,* and *M*; byte 7, the ASCII character *space*; and bytes 8–20 must contain the ASCII characters *C, O, N, F, I, G, U, R, A, T, I, O,* and *N*. Bytes 21–31 must contain an ASCII *space*. If this information is not entered correctly, the drive issues the message ILLEGAL COMMAND.

6.7.19.6 DisCache Parameters

PE – Prefetch Enable (Byte 32, Bit 1): When set to 1, this bit indicates that the drive will perform prefetching. A PE bit set to 0 indicates that no prefetching will occur. The CE bit (bit 0) must be set to 1 to enable use of the PE bit. The default value is 1.

CE – Cache Enable (Byte 32, Bit 0): When set to 1, this bit indicates that the drive will activate caching on all READ commands. With the CE bit set to 0, the drive will disable caching and use the 64K RAM only as a transfer buffer. The default setting is 1.

6.7.19.7 Number of Cache Segments (Byte 33)

This parameter indicates the number of segments the drive can index in the read cache—that is, the number of entries in the cache table. This byte is read-only and is dynamically adjusted by the drive.

6.7.19.8 Error Recovery Parameters

AWRE – Automatic Write Reallocation Enabled (Byte 36, Bit 7): When set to 1, indicates that the drive will enable automatic reallocation of bad blocks. Automatic Write Reallocation is similar to the function of Automatic Read Reallocation, but is initiated by the drive when a defective block has become inaccessible for writing. An AWRE bit set to 0 indicates that the Lightning 365/540/730AT will not automatically reallocate bad blocks. The default setting is 1.

ARR – Automatic Read Reallocation (Byte 36, Bit 6): When set to 1, this bit indicates that the drive will enable automatic reallocation of bad sectors. The drive initiates reallocation when the ARR bit is set to 1 and the drive encounters a hard error—that is, the same nonzero ECC syndrome occurs on two consecutive retries. The default setting is 1. When the ARR bit is set to 0, the drive will not perform automatic reallocation of bad sectors. If RC (byte 36, bit 4) is 1, the drive ignores this bit. The default value is 1.

RC – Read Continuous (Byte 36, Bit 4): When set to 1, this bit instructs the drive to transfer data of the requested length without adding delays to increase data integrity—that is, delays caused by the drive's error-recovery procedures. With RC set to 1 to maintain a continuous flow of data and avoid delays, the drive may send data that is erroneous. When the drive ignores an error, it does ***not*** post the error. The RC bit set to 0 indicates that potentially time-consuming operations for error recovery are acceptable during data transfer. The default setting is 0.

EEC – Enable Early Correction (Byte 36, Bit 3): When set to 1, this bit indicates that the drive will use its ECC algorithm if it detects two consecutive equal, nonzero error syndromes. The drive will not perform rereads before applying correction, unless it determines that the error is uncorrectable. An EEC bit set to 0 indicates that the drive will use its normal recovery procedure when an error occurs: rereads, followed by error correction. If the RC bit (byte 36, bit 4) is set to 1, the drive ignores the EEC bit. The default setting is 0.

DCR – Disable Early Correction (Byte 36, Bit 0): When set to 1, this bit indicates that all data will be transferred without correction, even if it would be possible to correct the data. A DCR bit set to 0 indicates that the data will be corrected if possible. If the data is uncorrectable, it will be transferred without correction, though the drive will attempt rereads. If RC (byte 36, bit 4) is set to 1, the drive ignores this bit. The default setting is 0. The drive will post all errors, whether DCR is set to 0 or 1.

NUMBER OF RETRIES (Byte 37): This byte specifies the number of times that the drive will attempt to recover from data errors by rereading the data, before it will apply correction. The drive performs rereads before ECC correction—unless EEC (byte 36, bit 3) is set to 1, enabling early correction. The default is eight.

ECC CORRECTION SPAN (Byte 38): This byte specifies the size, in bits, of the largest Read Data error on which the drive can attempt error correction. The value for this byte is fixed at 16.

6.7.19.9 Drive Parameters

AR – Auto Read (Byte 39, Bit 6): When this bit is set to 1, Auto Read is enabled. When the bit is set to 0, Auto Read is disabled. The default value is 1.

ACHS – Auto Cylinder, Head, Sector (Byte 39, Bit 5): When ACHS is set to 1, the hardware automatically updates the CHS value in the task file register. When the bit is 0, the CHS is not automatically updated. The default value is 1.

WCE – Write Cache Enable (Byte 39, Bit 2) : When this bit is set to 1, the Lightning 365/540/730AT hard disk enables the Write Cache. The host will terminate Write commands before data is completely written to the disk. When Write Caching is enabled, the WRITE command terminates when all of the data is transferred from the host to the buffer, even though all the data may not be written to the disk. Data continues to be written to the disk after the WRITE command terminates. If the following command is any command other than another WRITE command, the command is delayed until the remaining data is written to the disk. Upon completion, the new command continues normal execution. The default value is 1.

If the next command is another WRITE command, cached data continues to be written to the disk while new data is added to the buffer. The default setting is 1.

RUEE – Reallocate Uncorrectable Error Enables (Byte 39, Bit 1): When set to 1, this bit indicates that the Lightning 365/540/730AT hard disk drive will automatically reallocate uncorrectable hard errors, if the ARR bit (byte 36, bit 6) is set to 1. The default setting is 1.

6.8 ERROR REPORTING

At the start of a command's execution, the Lightning 365/540/730AT hard disk drive checks the Command Register for any conditions that would lead to an abort command error. The drive then attempts execution of the command. Any new error causes execution of the command to terminate at the point at which it occurred. Table 6-23 lists the valid errors for each command.

Table 6-23 *Command Errors*

COMMAND	**ERROR REGISTER**						**STATUS REGISTER**				
	BBK	**UNC**	**IDNF**	**ABRT**	**TKO**	**AMNF**	**DRDY**	**DWF**	**DSC**	**CORR**	**ERR**
Check Power Mode				V			V	V	V		V
Read Defect List	V	V	V	V		V	V	V	V	V	V
Execute Drive Diag.											V
Format Track			V	V			V	V	V		V
Identify Drive				V			V	V	V		V
Initialize Parameters							V	V	V		
Invalid Cmnd. Codes				V			V	V	V		V
Read Buffer				V			V	V	V		V
Read DMA	V	V	V	V		V	V	V	V	V	V
Read Configuration	V	V	V	V		V	V	V	V	V	V
Read Multiple	V	V	V	V		V	V	V	V	V	V
Read Sectors	V	V	V	V		V	V	V	V	V	V
Read Sectors Long	V		V	V		V	V	V	V		V
Read Verify Sectors	V	V	V	V		V	V	V	V	V	V
Recalibrate				V	V		V	V	V		V
Seek			V	V			V	V	V		V
Set Configuration	V		V	V			V	V	V		V
Set Features				V			V	V	V		V
Set Multiple Mode				V			V	V	V		V
Write Buffer				V			V	V	V		V
Write DMA	V		V	V			V	V	V		V
Write Multiple	V		V	V			V	V	V		V
Write Sectors	V		V	V			V	V	V		V
Write Sectors Long	V		V	V			V	V	V		V

Note:
V = Valid errors for each command
ABRT = Abort command error
AMNF = Data address mark not found error
BBK = Bad block detected
CORR = Corrected data error
DRDY = Drive ready
DSC = Disk seek complete not detected
DWF = Drive write fault detected
ERR = Error bit in the Status Register
IDNF = Requested ID not found
TK0 = Track zero not found error
UNC = Uncorrectable data error

GLOSSARY

A

ACCESS – (v) Read, write, or update information on some storage medium, such as a disk. (n) One of these operations.

ACCESS TIME – The interval between the time a request for data is made by the system and the time the data is available from the drive. Access time includes the actual seek time, rotational latency, and command processing overhead time. See also seek, rotational latency, and overhead.

ACTUATOR – Also known as the *positioned.* The internal mechanism that moves the read/write head to the proper track. The Quantum actuator consists of a rotary voice coil and the head mounting arms. One end of each head mounting arm attaches to the rotor with the read/write heads attached at the opposite end of each arm. As current is applied to the rotor, it rotates, positioning the heads over the desired cylinder on the media.

AIRLOCK – A patented Quantum feature that ensures durable and reliable data storage. Upon removal of power from the drive for any reason, the read/write heads automatically park and lock in a non data area called the landing zone. AIRLOCK allows the drive to withstand high levels of non-operating shock. When power is applied to the drive, airflow created from the spinning disks causes the AIRLOCK arm to swing back and unlock the actuator, allowing the heads to move from the landing zone. Upon power down, the AIRLOCK swings back to the locked position, locking the heads in the landing zone. A park utility is not required to park the heads on drives equipped with AIRLOCK (all Quantum drives).

ALLOCATION – The process of assigning particular areas of the disk to particular files. See also allocation unit.

ALLOCATION UNIT – An allocation unit, also known as a *cluster*, is a group of sectors on the disk that can be reserved for the use of a particular file.

AT – Acronym for Advanced Technology. Defined by IBM with the introduction of its third-generation personal computer called PC/AT. The term is now used in a generic sense for PCs that are compatible with the IBM PC and to refer to the system bus scheme.

AVERAGE SEEK TIME – The average time it takes for the read/write head to move to a specific location. To compute the average seek time, you divide the time it takes to complete a large number of random seeks all over the disk by the number of seeks performed.

B

BACKUP – A copy of a file, directory, or volume on a separate storage device from the original, for the purpose of retrieval in case the original is accidentally erased, damaged, or destroyed.

BAD BLOCK – A block (usually the size of a sector) that cannot reliably hold data because of a media flaw or damaged format markings.

BAD TRACK TABLE – A label affixed to the casing of a hard disk drive that tells which tracks are flawed and cannot hold data. The listing is typed into the low-level formatting program when the drive is being installed. Because Quantum hard disk drive's defect-management scheme handles all such flaws automatically, there is no need to concern yourself with bad track tables.

BEZEL – A plastic panel that extends the face of a drive so that it covers a computer's drive bay opening. The bezel usually contains a drive-activity LED. Also known as the *faceplate.*

BIOS – Acronym for Basic Input / Output System. The firmware portion of a computer that manages the flow of signals through the system bus and to the attached cards and peripheral devices.

BIT – Abbreviation for binary digit. A binary digit may have one of two values—1 or 0. This contrasts with a decimal digit, which may have a value from 0 to 9. A bit is one of the logic 1or logic 0 binary settings that make up a byte of data. See also byte.

BLOCK – A sector or group of sectors. By default, a block of data consists of 512 bytes.

BPI – Abbreviation for *bits per inch.* A measure of how densely information is packed on a storage medium. Flux changes per inch is also a term commonly used in describing storage density on a magnetic surface.

BUFFER – An area of RAM reserved for temporary storage of data that is waiting to be sent to a device that is not yet ready to receive it. The data is usually on its way to or from the hard disk drive or some other peripheral device.

BUS – The part of a chip, circuit board, or interface designed to send and receive data. The bus in a PC is on the motherboard, and contains plug-in slots for expansion cards.

BYTE – The basic unit of computer memory, large enough to hold one character of alphanumeric data. Comprised of eight bits. See also bit.

C

CACHE – Random-access memory (RAM) used as a buffer between the CPU and a hard disk. Information more likely to be read or changed is placed in the cache, where it can be accessed more quickly to speed up general data flow.

CAPACITY – The amount of information that can be stored on a hard disk drive. The data is stored in bytes, and capacity is usually expressed in megabytes.

CLEAN ROOM – An environmentally controlled dust-free assembly or repair facility in which hard disk drives are assembled or can be opened for internal servicing.

CLUSTER – A group of sectors on a hard disk drive that is addressed as one logical unit by the operating system.

CONTROLLER – Short form of *disk controller*. The chip or complete circuit that translates computer data and commands into a form suitable for use by the hard disk drive.

CONTROLLER CARD – An adapter holding the control electronics for one or more hard disks, usually installed in a slot in the computer.

CPU – Acronym for *Central Processing Unit*. The microprocessor chip that performs the bulk of data processing in a computer.

CRC – Acronym for *Cyclic Redundancy Check*. An error detection code that is recorded within each sector and is used to see whether parts of a string of data are missing or erroneous.

CYLINDER – On a hard disk drive that has more than one recording surface and heads that move to various tracks, the group of all tracks located at a given head position. The number of cylinders times the number of heads equals the number of tracks per drive.

D

DATA SEPARATOR – On a hard disk drive that stores data and timing information in an encoded form, the circuit that extracts the data from the combined data and clock signal.

DEDICATED SERVO – A surface separate from the surface used for data that contains only disk timing and positioning information and contains no data.

DEFECT MANAGEMENT – A method that is implemented to ensure long term data integrity. Defect management eliminates the need for user defect maps. This is accomplished by scanning the disk drives at the factory for defective sectors. Defective sectors are deallocated prior to shipment. In addition, during regular use, the drive continues to scan and compensate for any new defective sectors on the disk.

DISK – In general, any circular-shaped data-storage medium that stores data on the flat surface of the platter. The most common type of disk is the magnetic disk, which stores data as magnetic patterns in a metal or metal-oxide coating. Magnetic disks come in two forms: floppy and hard. Optical recording is a newer disk technology that gives higher capacity storage but at slower access times.

DISK CONTROLLER – A plug-in board, or embedded circuitry on the drive, that passes information to and from the disk. The Quantum hard disk drives all have controllers embedded on the drive printed-circuit board.

DMA – Acronym for *direct memory access*. A process by which data moves directly between a disk drive (or other device) and system memory without passing through the CPU, thus allowing the system to continue processing other tasks while the new data is being retrieved.

DOS – Acronym for *Disk Operating System*. The most common operating system used in IBM PCs. Manages all access to data on the disk.

DRIVE – Short form of *disk drive.*

DRIVE GEOMETRY – The functional dimensions of a drive in terms of the number of heads, cylinders, and sectors per track. See also logical format.

E

ECC – Acronym for *error correction code.* The recording of extra verifying information encoded along with the disk data. The controller uses the extra information to check for data errors, and corrects the errors when possible.

EISA – Acronym for *Extended Industry Standard Architecture.* Enhanced AT bus architecture designed by nine manufacturers of PC compatibles and announced in September 1988. EISA promises the advantages of IBM Micro Channel Architecture with the advantage of downward compatibility to the current standard AT bus, known as *ISA.*

EMBEDDED SERVO – A timing or location signal placed on the disk's surface on the tracks that also store data. These signals allow the actuator to fine-tune the position of the read/write heads.

ENCODING – The protocol by which particular data patterns are changed prior to being written on the disk surface as a pattern of On and Off or 1 and 0 signals.

EPROM – Acronym for *erasable programmable read only memory.* Integrated circuit memory chip that can store programs and data in a non volatile state. These devices can be erased by ultraviolet light and reused for new data.

EXTERNAL DRIVE – A drive mounted in an enclosure, separate from the PC or computer system enclosure, with its own power supply and fan, and connected to the system by a cable.

F

FAT – Acronym for *file allocation table.* A data table stored on the outer edge of a disk that tells the operating system which sectors are allocated to each file and in what order.

FCI – Acronym for *flux changes per inch.* See also BPI.

FILE SERVER – A computer that provides network stations with controlled access to shareable resources. The network operating system is loaded on the file server, and most shareable devices (disk subsystems, printers) are attached to it. The file server controls system security and monitors station-to-station communications. A dedicated file server can be used only as a file server while it is on the network. A non dedicated file server can be used simultaneously as a file server and a workstation.

FIRMWARE – The program instructions and data stored in an EPROM for use by a processor.

FLUX DENSITY – The number of magnetic field patterns that can be stored in a given length of disk surface. The number is usually stated as flux changes per inch (FCI), with typical values in the thousands.

FLYING HEIGHT – The distance between the read/write head and the disk surface caused by a cushion of air that keeps the head from contacting the media. Smaller flying heights permit more dense storage of data, but require more precise mechanical designs.

FORMAT – To write onto the disk surface a magnetic track pattern that specifies the locations of the tracks and sectors. This information must exist on a disk before it can store any user data. Formatting erases any previously stored data.

FORMATTED CAPACITY – The amount of room left to store data on the disk after the required space has been used to write sector headers, boundary definitions, and timing information generated by a format operation. All Quantum drive capacities are expressed in formatted capacity.

FORM FACTOR – The physical outer dimensions of a device as defined by industry standard. For example, most Quantum hard disk drives use a 3 1/2-inch form factor.

G

GIGABYTE (GB) – One billion bytes (one thousand megabytes).

GUIDE RAILS – Plastic strips attached to the sides of a hard disk drive mounted in an IBM AT and compatible computers so that the drive easily slides into place.

H

HALF HEIGHT – Term used to describe a drive that occupies half the vertical space of the original full size 5 1/4-inch drive. 1.625 inches high.

HARD DISK – A type of storage medium that retains data as magnetic patterns on a rigid disk, usually made of an iron oxide or alloy over a magnesium or aluminum platter. Because hard disks spin more rapidly than floppy disks, and the head flies closer to the disk, hard disks can transfer data faster and store more in the same volume.

HARD ERROR – A repeatable error in disk data that persists when the disk is reread, usually caused by defects in the media surface.

HEAD – The tiny electromagnetic coil and metal pole piece used to create and read back the magnetic patterns (write and read information) on the media.

HEAD CRASH – Damage to the read/write heads sometimes caused by contaminating dust, fingerprints, or smoke landing on the surface of the disk, or more often, by the heads striking the disk surface during operation.

HIGH-CAPACITY DRIVE – By industry conventions typically a drive of 100 megabytes or more.

HIGH-LEVEL FORMATTING – Formatting performed by the operating system's format program (for example, the DOS FORMAT program). Among other things, the formatting program creates the root directory and file allocation tables. See also low-level formatting.

HOME – Reference position track for recalibration of the actuator, usually the outer track (track 0).

HOST ADAPTER – A plug-in board that forms the interface between a particular type of computer system bus and the disk drive.

I

IDE – Acronym for i*ntegrated device electronics.* The term used for the interface on drives with embedded controllers that can be directly connected to the AT system bus. This connection can be through a 40-pin connector on the motherboard or an adapter board that contains only the drive-select decoding logic. Quantum AT drives use the IDE interface.

INITIALIZE – See low-level formatting.

INTERFACE – A hardware or software protocol, contained in the electronics of the disk controller and disk drive, that manages the exchange of data between the drive and computer.

INTERLEAVE – The arrangement of sectors on a track. A 1:1 interleave arranges the sectors so that the next sector arrives at the read/write heads just as the computer is ready to access it. See also interleave factor.

INTERLEAVE FACTOR – The number of sectors that pass beneath the read/write heads before the next numbered sector arrives. When the interleave factor is 3:1, a sector is read, two pass by, and then the next is read. It would take three revolutions of the disk to access a full track of data. Quantum drives have an interleave of 1:1, so a full track of data can be accessed within one revolution of the disk, thus offering the highest data throughput possible.

INTERNAL DRIVE – A drive mounted inside one of a computer's drive bays (or a hard disk on a card, which is installed in one of the computer's slots).

ISA – Acronym for *Industry Standard Architecture.* The standard 16 bit AT bus as designed by IBM for their PC/AT system. ISA has been the only industry standard bus for PCs until the recent release of MCA and EISA.

J

JUMPER – A tiny box that slips over two pins that protrude from a circuit board. When in place, the jumper connects the pins electrically. Some board manufacturers use Dual In-Line Package (DIP) switches instead of jumpers.

K

KILOBYTE (K) – A unit of measure consisting of 1,024 (2^{10}) bytes.

L

LANDING ZONE – A position inside the disk's inner cylinder in a non data area reserved as a place to rest the heads during the time that power is off. Using this area prevents the heads from touching the surface in data areas upon power down, adding to the data integrity and reliability of the disk drive.

LATENCY – The period of time during which the read/write heads are waiting for the data to rotate into position so that it can be accessed. Based on a disk rotation speed of 3,662 rpm, the maximum latency time is 16.4 milliseconds, and the average latency time is 8.2 milliseconds.

LOGICAL FORMAT – The logical drive geometry that appears to an AT system BIOS as defined by the drive tables and stored in CMOS. With an installation program like Disk Manager, the drive can be redefined to any logical parameters necessary to adapt to the system drive tables.

LOOK AHEAD – The technique of buffering data into cache RAM by reading subsequent blocks in advance to anticipate the next request for data. The look ahead technique speeds up disk access of sequential blocks of data.

LOW-LEVEL FORMATTING – Formatting that creates the sectors on the platter surfaces so the operating system can access the required areas for generating the file structure. Quantum drives are shipped with the low-level formatting already done.

LOW PROFILE – Describes drives built to the 3 1/2-inch form factor, which are only 1 inch high. The standard form factor drives are 1.625 inches high.

M

MB – See megabyte.

MEDIA – The magnetic film that is deposited or coated on an aluminum substrate which is very flat and in the shape of a disk. The media is overcoated with a lubricant to prevent damage to the heads or media during head take off and landing. The media is where the data is stored inside the disk in the form of magnetic flux or polarity changes.

MEGABYTE (MB) – A unit of measurement equal to 1,024 kilobytes, or 1,048,576 bytes except when referring to disk storage capacity.

1 MB = 1,000,000 bytes when referring to disk storage capacity.

See also kilobyte.

MEGAHERTZ – A measurement of frequency in millions of cycles per second.

MHz – See megahertz.

MICROPROCESSOR – The integrated circuit chip that performs the bulk of data processing and controls the operation of all of the parts of the system. A disk drive also contains a microprocessor to handle all of the internal functions of the drive and to support the embedded controller.

MICROSECOND (µs) – One millionth of a second (.000001 sec.).

MILLISECOND (ms) – One thousandth of a second (.001 sec.).

MTBF – Mean Time Between Failure. Used as a reliability rating to determine the expected life of the product expressed in power on hours (POH). There are several accepted methods for calculating this value that produce very different results and generate much confusion in the industry. When comparing numbers you should first verify which method was used to calculate the values.

MTTR – Mean Time To Repair. The average time it takes to repair a drive that has failed for some reason. This only takes into consideration the changing of the major sub-assemblies such as circuit board or sealed housing. Component level repair is not included in this number as this type of repair is not performed in the field.

O

OVERHEAD – The processing time of a command by the controller, host adapter or drive prior to any actual disk accesses taking place.

OVERWRITE – To write data on top of existing data, erasing it.

OXIDE – A metal-oxygen compound. Most magnetic coatings are combinations of iron or other metal oxides, and the term has become a general one for the magnetic coating on tape or disk.

P

PARTITION – A portion of a hard disk devoted to a particular operating system and accessed as one logical volume by the system.

PERFORMANCE – A measure of the speed of the drive during normal operation. Factors affecting performance are seek times, transfer rate and command overhead.

PERIPHERAL – A device added to a system as an enhancement to the basic CPU, such as a disk drive, tape drive or printer.

PHYSICAL FORMAT – The actual physical layout of cylinders, tracks, and sectors on a disk drive.

PLATED MEDIA – Disks that are covered with a hard metal alloy instead of an iron-oxide compound. Plated disks can store greater amounts of data in the same area as a coated disk.

PLATTER – A disk made of metal (or other rigid material) that is mounted inside a fixed disk drive. Most drives use more than one platter mounted on a single spindle (shaft) to provide more data storage surfaces in a small package. The platter is coated with a magnetic material that is used to store data as transitions of magnetic polarity.

POH – Acronym for *power on hours.* The unit of measurement for Mean Time Between Failure as expressed in the number of hours that power is applied to the device regardless of the amount of actual data transfer usage. See MTBF.

POSITIONER – See actuator.

PROGRAMMED I/0 – The method by which an AT system transfers data between the system and disk drive through control of the system BIOS. Programmed I/O requires the system microprocessor to perform all of the transfer operations.

R

RAM – Acronym for *random access memory.* An integrated circuit memory chip which allows information to be stored and retrieved by a microprocessor or controller. The information may be stored and retrieved in any order desired, and the address of one storage location is as readily accessible as any other.

RAM DISK – A "phantom disk drive" for which a section of system memory (RAM) is set aside to hold data, just as if it were a number of disk sectors. The access to this data is extremely fast but is lost when the system is reset or turned off.

READ AFTER WRITE – A mode of operation that has the computer read back each sector on the disk, checking that the data read back is the same as recorded. This slows disk operations, but raises reliability.

READ VERIFY – A disk mode where the disk reads in data to the controller, but the controller only checks for errors and does not pass the data on to the system.

READ/WRITE HEAD – The tiny electromagnetic coil and metal pole piece used to create and read back the magnetic patterns (write or read information) on the disk. Each side of each platter has its own read/write head.

REMOVABLE DISK – Generally said of disk drives where the disk itself is meant to be removed, and in particular of hard disks using disks mounted in cartridges. Their advantage is that multiple disks can be used to increase the amount of stored material, and that once removed, the disk can be stored away to prevent unauthorized use.

RLL – Run Length Limited. A method used on some hard disks to encode data into magnetic pulses. RLL requires more processing, but stores almost 50% more data per disk than the MFM method.

ROM – Acronym for *read only memory.* Usually in the form of an EPROM that contains data or programs that can be accessed and read but not modified by the system.

ROTARY ACTUATOR – The rotary actuator replaces the stepper motor used in the past by many hard disk manufacturers. The rotary actuator is perfectly balanced and rotates around a single pivot point. It allows closed-loop feedback positioning of the heads, which is more accurate than stepper motors.

ROTATIONAL LATENCY – The delay between when the controller starts looking for a specific block of data on a track and when that block rotates around to where it can be read by the read/write head. On the average, it is half of the time needed for a full rotation (about 8 ms.).

S

SCSI – Acronym for *Small Computer System Interface*, an American National Standards Institute (ANSI) version of Shugart Associates' SASI interface between the computer and controller. SCSI has grown in popularity and is one of the most flexible and intelligent interfaces available.

SECTOR – A section of space along a track on the disk, or the data that is stored in that section. Hard disks most often have sectors that are 512 data bytes long plus several bytes overhead for error correcting codes. Each sector is preceded by ID data known as a header, which cannot be overwritten.

SEEK – A movement of the disk read/write head in or out to a specific track.

SERVO DATA – Magnetic markings written on the media that guide the read/write heads to the proper position.

SERVO SURFACE – A separate surface containing only positioning and disk timing information but no data.

SETTLE TIME – The interval between when a track to track movement of the head stops, and when the residual vibration and movement dies down to a level sufficient for reliable reading or writing.

SHOCK RATING – A rating (expressed in Gs) of how much shock a disk drive can sustain without damage.

SOFT ERROR – An error in reading data from the disk that does not recur if the same data is reread. Often caused by power fluctuations or noise spikes.

SOFT SECTORED – Disks that mark the beginning of each sector of data within a track by a magnetic pattern.

SPINDLE – The center shaft of the disk upon which the drive's platters are mounted.

SPUTTER – A type of coating process used to apply the magnetic coating to some high-performance disks. In sputtering, the disks are placed in a vacuum chamber and the coating is vaporized and deposited on the disks. The resulting surface is hard, smooth, and capable of storing data at high density. Quantum disk drives use sputtered thin film disks.

STEPPER – A type of motor that moves in discrete amounts for each input electrical pulse. Stepper motors used to be widely used for read/write head positioners, since they can be geared to move the head one track per step. Stepper motors are not as fast or reliable as the rotary voice coil actuators which Quantum disk drives use.

SUBSTRATE – The material the disk platter is made of beneath the magnetic coating. Hard disks are generally made of aluminum or magnesium alloy (or glass, for optical disks) while the substrate of floppies is usually mylar.

SURFACE – The top or bottom side of the platter which is coated with the magnetic material for recording data. On some drives one surface may be reserved for positioning information.

T

THIN FILM – A type of coating, used for both disk surfaces and read/write heads. Thin film surfaces allow more bits to be stored per disk.

TPI – Acronym for *tracks per inch.* The number of tracks or cylinders that are written in each inch of travel across the surface of a disk.

TRACK – One of the many concentric magnetic circle patterns written on a disk surface as a guide to where to store and read the data.

TRACK DENSITY – How closely the tracks are packed on a disk surface. The number is specified as tracks per inch (TPI).

TRACK TO TRACK SEEK TIME – The time required for the read/write heads to move to an adjacent track.

TRANSFER RATE – The rate at which the disk sends and receives data from the controller. Drive specifications usually reference a high number that is the burst mode rate for transferring data across the interface from the disk buffer to system RAM. Sustained data transfer is at a much lower rate because of system processing overhead, head switches, and seeks.

U

UNFORMATTED CAPACITY – The total number of bytes of data that could be fit onto a disk. Formatting the disk requires some of this space to record location, boundary definitions, and timing information. After formatting, user data can be stored on the remaining disk space, known as formatted capacity. The size of a Quantum drive is expressed in formatted capacity.

V

VOICE COIL – A type of motor used to move the disk read/write head in and out to the right track. Voice-coil actuators work like loudspeakers with the force of a magnetic coil causing a proportionate movement of the head. Quantum's actuator uses voice-coil technology, and thereby eliminates the high stress wearing parts found on stepper motor type actuators.

W

WEDGE SERVO – The position on every track that contains data used by the closed loop positioning control. This information is used to fine tune the position of the read/write heads exactly over the track center.

WINCHESTER DISKS – Hard disks that use a technology similar to an IBM model using Winchester as the code name. These disks use read/write heads that ride just above the magnetic surface, held up by the air flow created by the turning disk. When the disk stops turning, the heads land on the surface, which has a specially lubricated coating. Winchester disks must be sealed and have a filtration system since ordinary dust particles are large enough to catch between the head and the disk.

WRITE ONCE – In the context of optical disks, technologies that allow the drive to store data on a disk and read it back, but not to erase it.

X

XT – On the bus level, the original 8-bit version of what is now the AT bus.

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